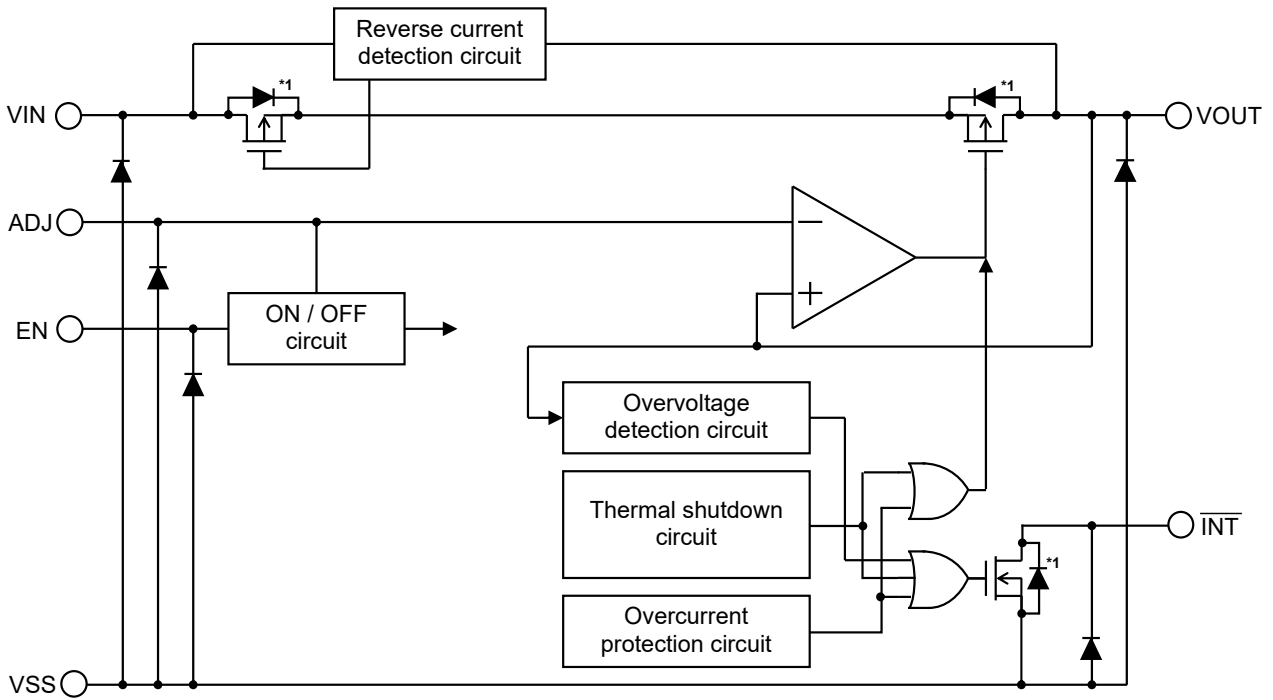




■ **Block Diagrams**

1. **S-19721 Series A type**



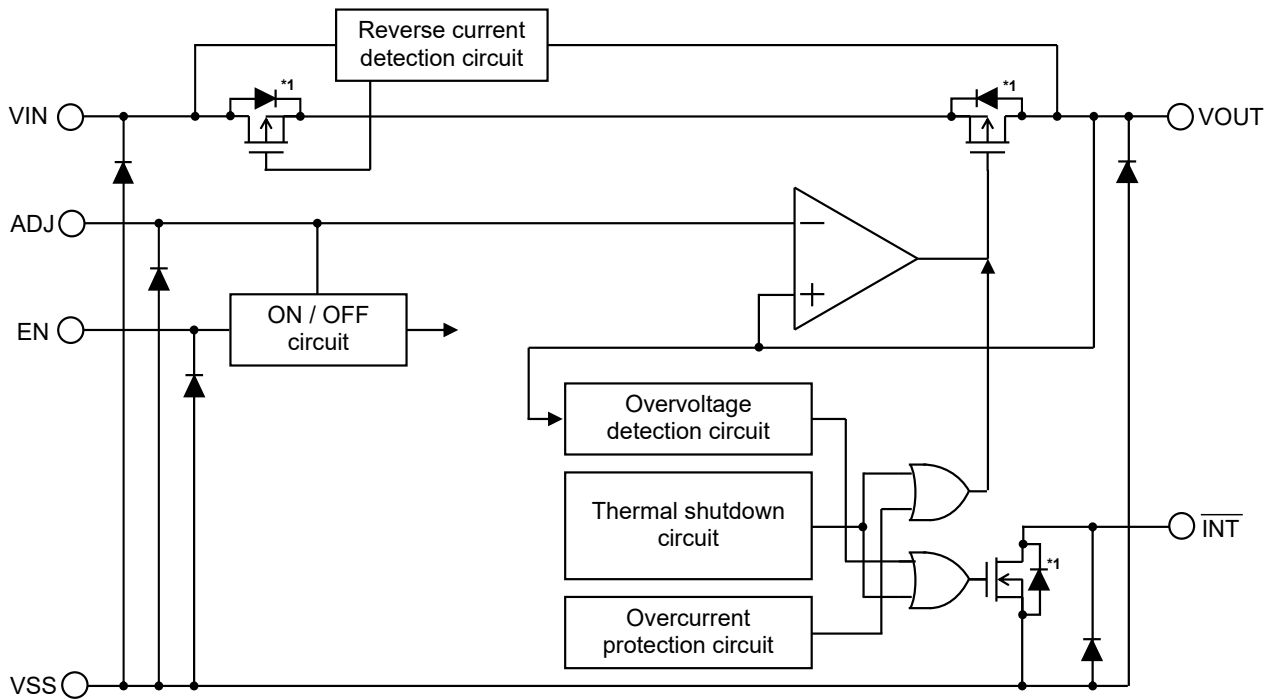
\*1. Parasitic diode

Figure 1

Table 1 Anomaly Notification Function

Overvoltage Monitoring	Ground Fault Monitoring	Overheat Monitoring
Available	Available	Available

2. S-19721 Series B type



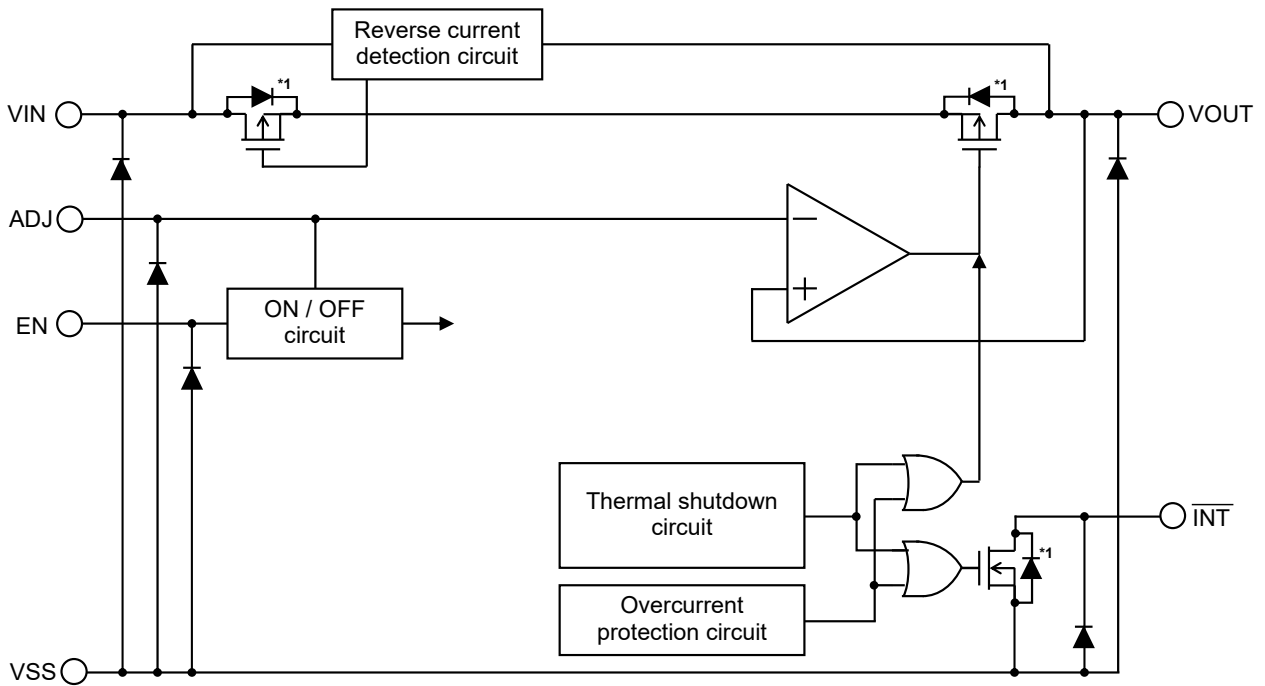
\*1. Parasitic diode

Figure 2

Table 2 Anomaly Notification Function

Overvoltage Monitoring	Ground Fault Monitoring	Overheat Monitoring
Available	Unavailable	Available

**3. S-19721 Series C type**



\*1. Parasitic diode

**Figure 3**

**Table 3 Anomaly Notification Function**

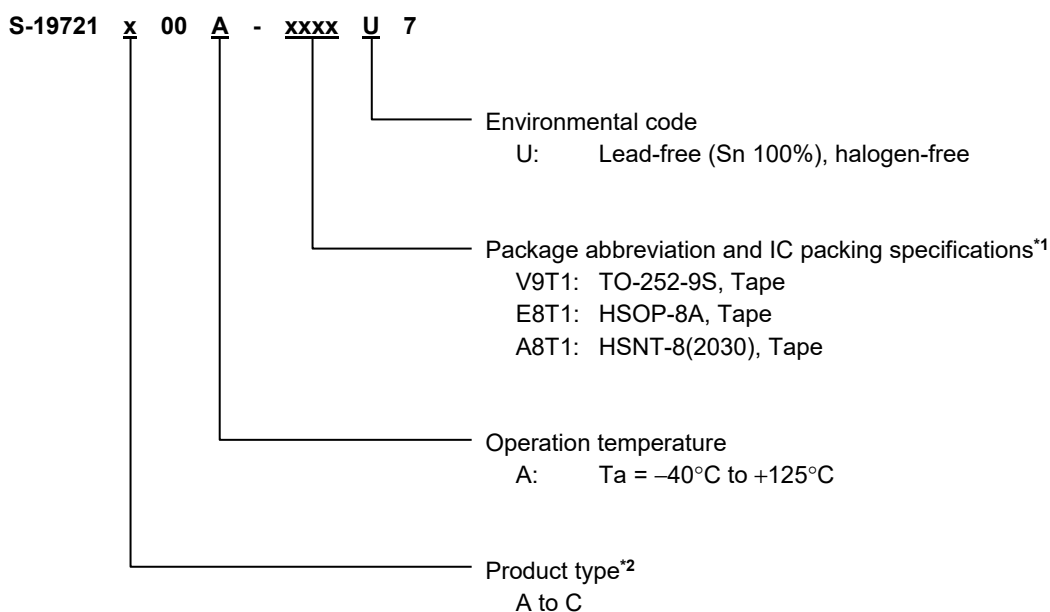
Overvoltage Monitoring	Ground Fault Monitoring	Overheat Monitoring
Unavailable	Available	Available

## ■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 1.  
 Contact our sales representatives for details of AEC-Q100 reliability specification.

## ■ Product Name Structure

### 1. Product name



\*1. Refer to the tape drawing.

\*2. Refer to "2. Function list of product types".

### 2. Function list of product types

Table 4

Product Type	Anomaly Notification Function		
	Overtoltage Monitoring	Ground Fault Monitoring	Overheat Monitoring
A	Available	Available	Available
B	Available	Unavailable	Available
C	Unavailable	Available	Available

### 3. Packages

Table 5 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
TO-252-9S	VA009-A-P-SD	VA009-A-C-SD	VA009-A-R-SD	VA009-A-L-SD
HSOP-8A	FH008-A-P-SD	FH008-A-C-SD	FH008-A-R-SD	FH008-A-L-SD
HSNT-8(2030)	PP008-A-P-SD	PP008-A-C-SD	PP008-A-R-SD	PP008-A-L-SD

**4. Product name list**

**4.1 S-19721 Series A type**

**Table 6**

TO-252-9S	HSOP-8A	HSNT-8(2030)
S-19721A00A-V9T1U7	S-19721A00A-E8T1U7	S-19721A00A-A8T1U7

**4.2 S-19721 Series B type**

**Table 7**

TO-252-9S	HSOP-8A	HSNT-8(2030)
S-19721B00A-V9T1U7	S-19721B00A-E8T1U7	S-19721B00A-A8T1U7

**4.3 S-19721 Series C type**

**Table 8**

TO-252-9S	HSOP-8A	HSNT-8(2030)
S-19721C00A-V9T1U7	S-19721C00A-E8T1U7	S-19721C00A-A8T1U7

## Pin Configurations

### 1. TO-252-9S

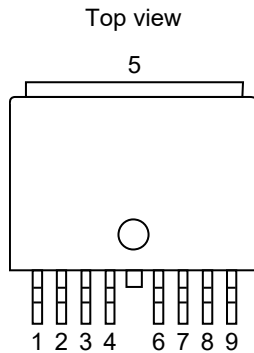


Figure 4

Table 9

Pin No.	Symbol	Description
1	VOUT	Output voltage pin
2	NC*1	No connection
3	NC*1	No connection
4	INT	Anomaly notification signal output pin
5	VSS	GND pin
6	ADJ	Output voltage adjustment pin
7	EN	Enable pin
8	NC*1	No connection
9	VIN	Input voltage pin

- \*1. The NC pin is electrically open.  
 The NC pin can be connected to the VIN pin or the VSS pin.

### 2. HSOP-8A

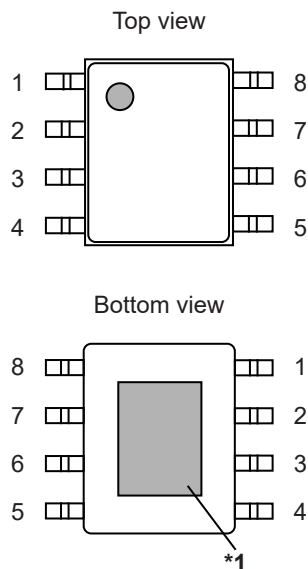


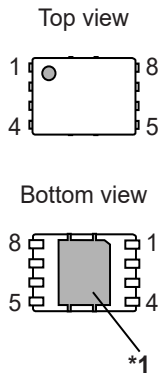
Figure 5

Table 10

Pin No.	Symbol	Description
1	VOUT	Output voltage pin
2	NC*2	No connection
3	VSS	GND pin
4	INT	Anomaly notification signal output pin
5	ADJ	Output voltage adjustment pin
6	VSS	GND pin
7	EN	Enable pin
8	VIN	Input voltage pin

- \*1. Connect the heat sink of backside at shadowed area to the board, and set electric potential GND.  
 However, do not use it as the function of electrode.
- \*2. The NC pin is electrically open.  
 The NC pin can be connected to the VIN pin or the VSS pin.

**3. HSNT-8(2030)**



**Figure 6**

**Table 11**

Pin No.	Symbol	Description
1	VOUT	Output voltage pin
2	NC*2	No connection
3	VSS	GND pin
4	$\overline{\text{INT}}$	Anomaly notification signal output pin
5	ADJ	Output voltage adjustment pin
6	VSS	GND pin
7	EN	Enable pin
8	VIN	Input voltage pin

- \*1. Connect the heat sink of backside at shadowed area to the board, and set electric potential GND. However, do not use it as the function of electrode.
- \*2. The NC pin is electrically open.  
The NC pin can be connected to the VIN pin or the VSS pin.



## ■ Absolute Maximum Ratings

Table 12

(Ta = +25°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit
Input voltage	V <sub>IN</sub>	V <sub>SS</sub> – 0.3 to V <sub>SS</sub> + 45.0	V
	V <sub>ADJ</sub>	V <sub>SS</sub> – 0.3 to V <sub>SS</sub> + 45.0	V
	V <sub>EN</sub>	V <sub>SS</sub> – 0.3 to V <sub>SS</sub> + 45.0	V
Output voltage	V <sub>OUT</sub>	V <sub>SS</sub> – 0.3 to V <sub>SS</sub> + 45.0	V
	V <sub>INT</sub>	V <sub>SS</sub> – 0.3 to V <sub>SS</sub> + 45.0	V
Output current	I <sub>OUT</sub>	325	mA
Junction temperature	T <sub>J</sub>	–40 to +150	°C
Operation ambient temperature	T <sub>opr</sub>	–40 to +125	°C
Storage temperature	T <sub>stg</sub>	–40 to +150	°C

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

## ■ Thermal Resistance Value

Table 13

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
Junction-to-ambient thermal resistance*1	θ <sub>JA</sub>	TO-252-9S	Board A	–	88	–	°C/W
			Board B	–	63	–	°C/W
			Board C	–	37	–	°C/W
			Board D	–	31	–	°C/W
			Board E	–	28	–	°C/W
		HSOP-8A	Board A	–	104	–	°C/W
			Board B	–	74	–	°C/W
			Board C	–	39	–	°C/W
			Board D	–	37	–	°C/W
			Board E	–	31	–	°C/W
		HSNT-8(2030)	Board A	–	181	–	°C/W
			Board B	–	135	–	°C/W
			Board C	–	40	–	°C/W
			Board D	–	42	–	°C/W
			Board E	–	32	–	°C/W

\*1. Test environment: compliance with JEDEC STANDARD JESD51-2A

**Remark** Refer to "■ Power Dissipation" and "Test Board" for details.

## ■ Recommended Operation Conditions

Table 14

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
V <sub>IN</sub> pin voltage	V <sub>IN</sub>	–	4.0	–	36	V
ADJ pin voltage*1	V <sub>ADJ</sub>	–	2.0	–	8.0	V
EN pin voltage	V <sub>EN</sub>	–	0.0	–	V <sub>ADJ</sub>	V
Output current*2	I <sub>OUT</sub>	–	0.1	–	250	mA
Input capacitor	C <sub>IN</sub>	–	4.7	–	–	μF
Output capacitor	C <sub>L</sub>	–	4.7	–	1000	μF
	ESR	–	–	–	3	Ω
External pull-up resistor for INT pin	R <sub>INT</sub>	–	3	–	–	kΩ

\*1. Please contact our sales representatives when using V<sub>ADJ</sub> > 8.0 V.

\*2. Due to limitation of the power dissipation, this value may not be satisfied. Attention should be paid to the power dissipation when the output current is large.

■ **Electrical Characteristics**

**Table 15**

( $V_{IN} = 13.5\text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$  unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit	
Offset voltage*1	$\Delta V_{OUT}$	$2.0\text{ V} \leq V_{ADJ} \leq V_{IN} - 2.0\text{ V}$ , $V_{ADJ} \leq 8.0\text{ V}$ *5	$4.0\text{ V} \leq V_{IN} \leq 22.0\text{ V}$ , $0.1\text{ mA} \leq I_{OUT} \leq 250\text{ mA}$	-4.5	-	+4.5	mV	1
			$4.0\text{ V} \leq V_{IN} \leq 36.0\text{ V}$ , $0.1\text{ mA} \leq I_{OUT} \leq 125\text{ mA}$	-4.5	-	+4.5	mV	1
Dropout voltage*2	$V_{drop}$	$V_{ADJ} \geq 4.0\text{ V}$ , $I_{OUT} = 125\text{ mA}$	-	330	630	mV	2	
Line regulation*3	$\Delta V_{OUT1}$	$6.0\text{ V} \leq V_{IN} \leq 36.0\text{ V}$ , $I_{OUT} = 10\text{ mA}$ , $V_{ADJ} = 5.0\text{ V}$	-	-	4.5	mV	2	
Load regulation*4	$\Delta V_{OUT2}$	$0.1\text{ mA} \leq I_{OUT} \leq 250\text{ mA}$ , $V_{ADJ} = 5.0\text{ V}$	-	-	4.5	mV	2	
Input voltage	$V_{IN}$	-	4.0	-	36.0	V	-	
Current consumption during operation	$I_{SS1}$	$V_{ADJ} = 5.0\text{ V}$ , $I_{OUT} = 0.01\text{ mA}$ , $I_{SS1} = I_{IN} - I_{OUT}$	-	40	60	$\mu\text{A}$	3	
Reverse current	$I_{REV}$	$V_{IN} = 0\text{ V}$ , $V_{ADJ} = 5.0\text{ V}$ , $V_{OUT} = 16.0\text{ V}$	-5	0	-	$\mu\text{A}$	4	
Current consumption during power-off	$I_{SS2}$	$V_{ADJ} = 0\text{ V}$	-	3.7	9.9	$\mu\text{A}$	5	
EN pin input voltage "H"	$V_{ENH}$	Determined by $V_{OUT}$ output level	2.0	-	-	V	6	
EN pin input voltage "L"	$V_{ENL}$	Determined by $V_{OUT}$ output level	-	-	0.5	V	6	
EN pin input current "H"	$I_{ENH}$	$V_{EN} = 5.0\text{ V}$	-0.1	-	0.5	$\mu\text{A}$	6	
EN pin input current "L"	$I_{ENL}$	$V_{EN} = 0\text{ V}$	-0.1	-	0.1	$\mu\text{A}$	6	
ADJ pin input voltage "H"	$V_{ADJH}$	Determined by $V_{OUT}$ output level	2.0	-	-	V	7	
ADJ pin input voltage "L"	$V_{ADJL}$	Determined by $V_{OUT}$ output level	-	-	0.5	V	7	
ADJ pin input current "H"	$I_{ADJH}$	$V_{ADJ} = 5.0\text{ V}$	-0.1	-	2.0	$\mu\text{A}$	7	
ADJ pin input current "L"	$I_{ADJL}$	$V_{ADJ} = 0\text{ V}$	-0.1	-	0.1	$\mu\text{A}$	7	
Ripple rejection	$ RR $	$f = 100\text{ Hz}$ , $\Delta V_{rip} = 0.5\text{ V}_{pp}$ , $I_{OUT} = 5\text{ mA}$	-	80	-	dB	8	
Limit current	$I_{LIM}$	$V_{IN} = 7.0\text{ V}$ , $V_{ADJ} = 5.0\text{ V}$ , $V_{OUT} = V_{ADJ} \times 0.85$ , $T_a = +25^\circ\text{C}$	350	500	700	mA	9	
Short-circuit current	$I_{short}$	$V_{IN} = 7.0\text{ V}$ , $V_{ADJ} = 5.0\text{ V}$ , $V_{OUT} = 0\text{ V}$ , $T_a = +25^\circ\text{C}$	350	500	700	mA	9	
Ground fault detection current	$I_{LIMD}$	A/C type, $V_{IN} = 7.0\text{ V}$ , $V_{ADJ} = 5.0\text{ V}$ , $T_a = +25^\circ\text{C}$	250	-	$I_{LIM}$	mA	10	
Thermal shutdown detection temperature	$T_{SD}$	Junction temperature	-	175	-	$^\circ\text{C}$	-	
Thermal shutdown release temperature	$T_{SR}$	Junction temperature	-	165	-	$^\circ\text{C}$	-	
Overvoltage detection voltage	$V_{OVD}$	A/B type, $V_{IN} = V_{ADJ} + 2.0\text{ V}$ , $V_{ADJ} = 5.0\text{ V}$	$V_{ADJ} + 0.05$	$V_{ADJ} + 0.09$	$V_{ADJ} + 0.12$	V	-	
$\overline{\text{INT}}$ pin output voltage "L"	$V_{OL,\overline{\text{INT}}}$	$V_{PU} = 5.0\text{ V}$ , $R_{\overline{\text{INT}}} = 3.0\text{ k}\Omega$	-	-	0.4	V	11	
$\overline{\text{INT}}$ pin leakage current	$I_{LEAK,\overline{\text{INT}}}$	$V_{\overline{\text{INT}}} = 5.0\text{ V}$	-	-	2.0	$\mu\text{A}$	12	
$\overline{\text{INT}}$ pin "H" output delay time	$t_{dH,\overline{\text{INT}}}$	$V_{PU} = 5.0\text{ V}$ , $R_{\overline{\text{INT}}} = 3.0\text{ k}\Omega$	-	250	-	$\mu\text{s}$	-	

\*1. Indicates the difference between output voltage ( $V_{OUT}$ ) and ADJ pin voltage ( $V_{ADJ}$ ).

The accuracy is guaranteed when the input voltage, output current, and temperature satisfy the conditions listed above.

$$\Delta V_{OUT} = V_{OUT} - V_{ADJ}$$

\*2. Indicates the difference between input voltage ( $V_{IN1}$ ) and the output voltage when the output voltage becomes 98% of the output voltage value ( $V_{OUT3}$ ) after the input voltage ( $V_{IN}$ ) is decreased gradually.

$$V_{drop} = V_{IN1} - (V_{OUT3} \times 0.98)$$

$V_{OUT3}$ : Output voltage value at  $V_{IN} = V_{ADJ} + 2.0\text{ V}$ , and  $I_{OUT} = 125\text{ mA}$

\*3. Indicates the dependency of the output voltage against the input voltage. The value shows how much the output voltage changes due to a change in the input voltage after fixing output current constant.

\*4. Indicates the dependency of the output voltage against the output current. The value shows how much the output voltage changes due to a change in the output current after fixing input voltage constant.

\*5. Please contact our sales representatives when using  $V_{ADJ} > 8.0\text{ V}$ .

■ Test Circuits

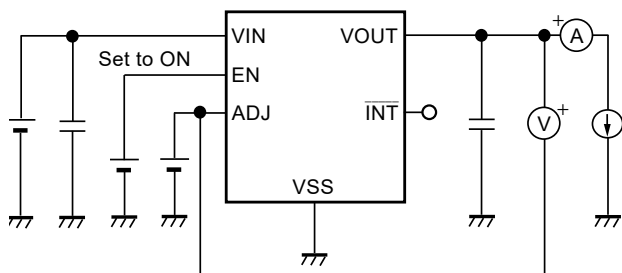


Figure 7 Test Circuit 1

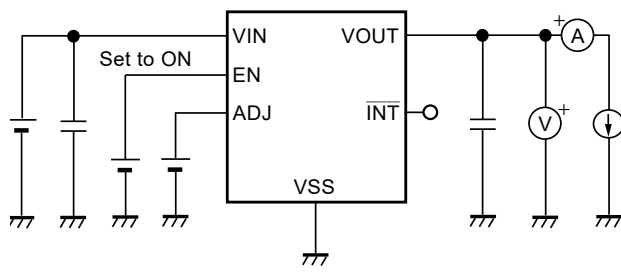


Figure 8 Test Circuit 2

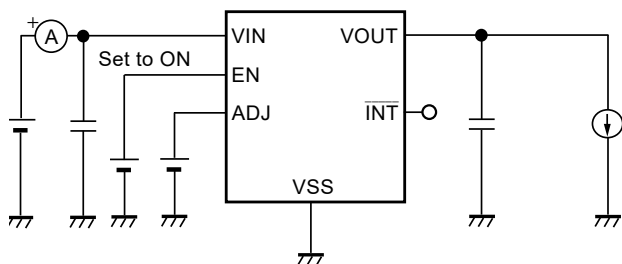


Figure 9 Test Circuit 3

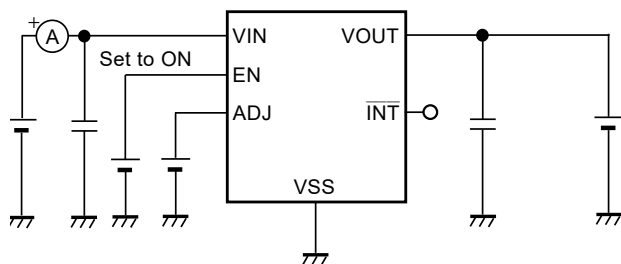


Figure 10 Test Circuit 4

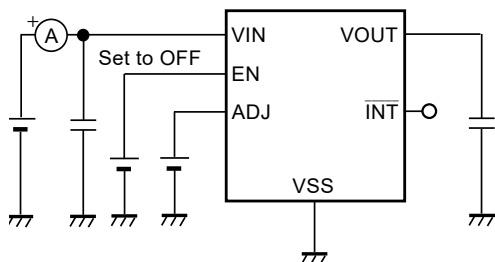


Figure 11 Test Circuit 5

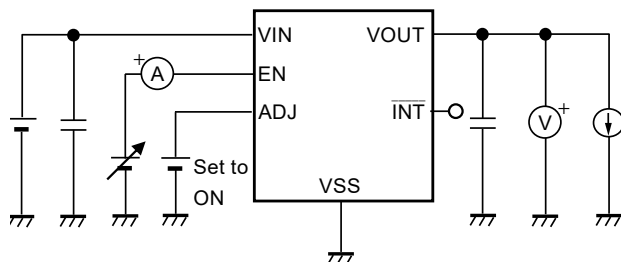


Figure 12 Test Circuit 6

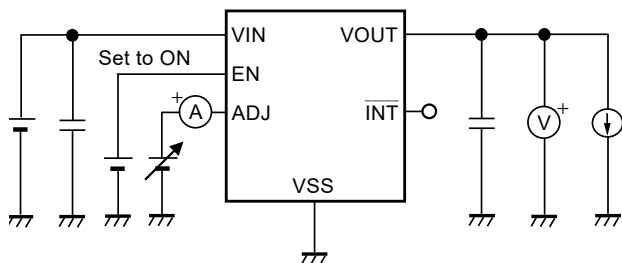


Figure 13 Test Circuit 7

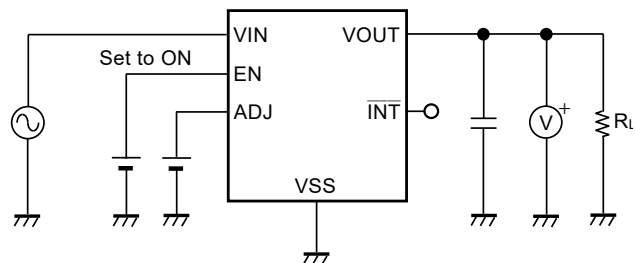


Figure 14 Test Circuit 8

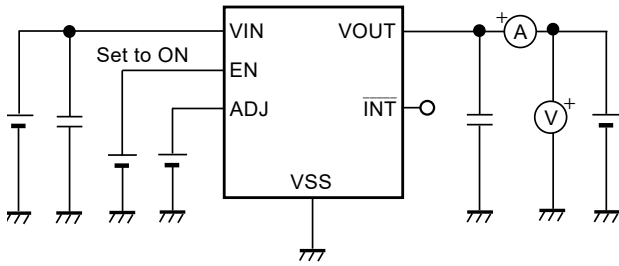


Figure 15 Test Circuit 9

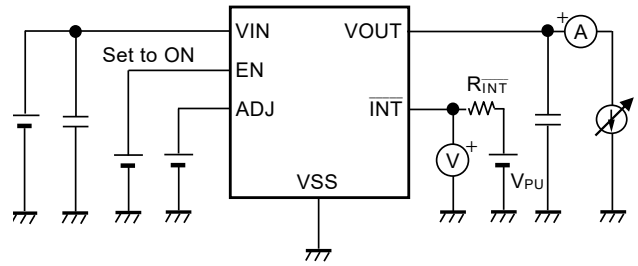


Figure 16 Test Circuit 10

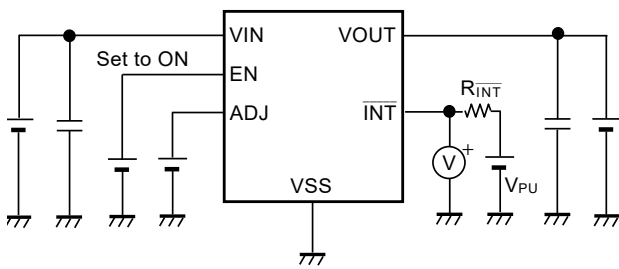


Figure 17 Test Circuit 11

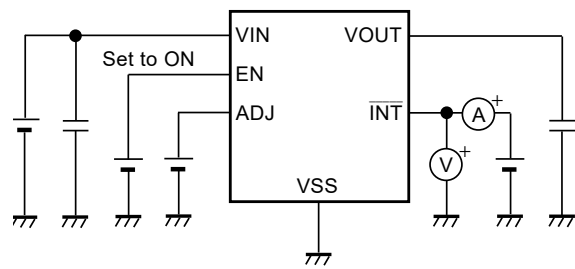
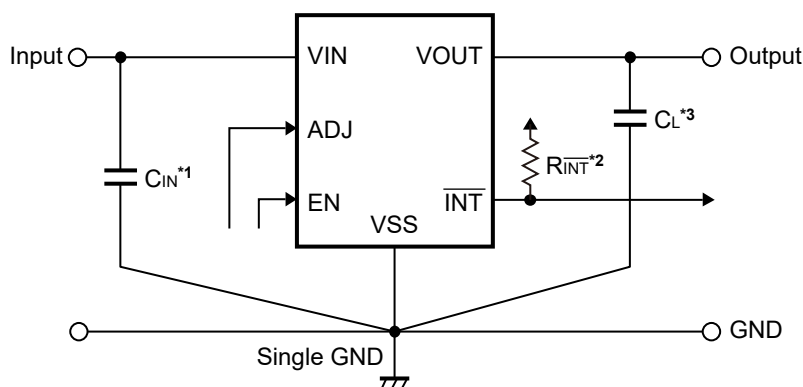


Figure 18 Test Circuit 12

## ■ Standard Circuit



- \*1.  $C_{IN}$  is a capacitor for stabilizing the input.
- \*2.  $R_{INT}$  is the external pull-up resistor for the  $\overline{INT}$  pin.
- \*3.  $C_L$  is a capacitor for stabilizing the output.

Figure 19

**Caution** The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using an actual application to set the constants.

## ■ Condition of Application

- Input capacitor ( $C_{IN}$ ): A ceramic capacitor with capacitance of 4.7  $\mu\text{F}$  or more is recommended.  
 Output capacitor ( $C_L$ ): A ceramic capacitor with capacitance of 4.7  $\mu\text{F}$  to 1000  $\mu\text{F}$  is recommended.

**Caution** Generally, in a voltage tracker, an oscillation may occur depending on the selection of the external parts. Perform thorough evaluation including the temperature characteristics with an actual application using the above capacitors to confirm no oscillation occurs.

## ■ Selection of Input Capacitor ( $C_{IN}$ ) and Output Capacitor ( $C_L$ )

This IC requires  $C_L$  between the VOUT pin and the VSS pin for phase compensation. The operation is stabilized by a ceramic capacitor with capacitance of 4.7  $\mu\text{F}$  to 1000  $\mu\text{F}$  over the entire temperature range. When using an OS capacitor, a tantalum capacitor or an aluminum electrolytic capacitor, the capacitance also must be 4.7  $\mu\text{F}$  to 1000  $\mu\text{F}$ .

However, an oscillation may occur depending on the equivalent series resistance (ESR).

Moreover, this IC requires  $C_{IN}$  between the VIN pin and the VSS pin for a stable operation.

Generally, an oscillation may occur when a voltage tracker is used under the condition that the impedance of the power supply is high.

Note that the output voltage transient characteristics varies depending on the capacitance of  $C_{IN}$  and  $C_L$  and the value of ESR.

**Caution** Perform thorough evaluation including the temperature characteristics with an actual application to select  $C_{IN}$  and  $C_L$ .

## ■ Operation

### 1. Basic operation

Figure 20 shows the block diagram of this IC to describe the basic operation.

The error amplifier compares the output voltage ( $V_{OUT}$ ) with the ADJ pin voltage ( $V_{ADJ}$ ).

The error amplifier controls the output transistor to keep  $V_{OUT}$  equal to  $V_{ADJ}$  without being affected by the input voltage ( $V_{IN}$ ), that is, the tracking operation is performed.

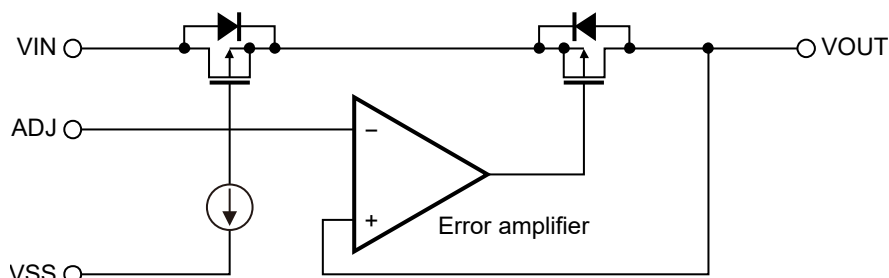


Figure 20

### 2. Output transistor

In this IC, a low on-resistance P-channel MOS FET is used between the VIN pin and the VOUT pin as the output transistor. In order to maintain the tracking operation of  $V_{ADJ}$  and  $V_{OUT}$ , the on-resistance of the output transistor varies appropriately according to the output current ( $I_{OUT}$ ).

Also, the reverse current prevention transistor is connected in series with the output transistor.

### 3. ADJ pin, EN pin

The ADJ pin and EN pin control the internal circuit and the output transistor in order to start and stop the tracker.

When the ADJ pin or EN pin is set to ON ( $V_{ADJ} \geq V_{ADJH}$ ,  $V_{EN} \geq V_{ENH}$ ), the tracking operation starts and  $V_{OUT}$  is adjusted so that it becomes equal to  $V_{ADJ}$ .

When the ADJ pin is set to OFF ( $V_{ADJ} \leq V_{ADJL}$ ) or the EN pin is set to OFF ( $V_{EN} \leq V_{ENL}$ ), the internal circuit stops operating and the output transistor between the VIN pin and the VOUT pin is turned off, reducing current consumption significantly (power-off status).

The ADJ pin or the EN pin is internally pulled down to the VSS pin in the floating status, so the VOUT pin is set to the  $V_{SS}$  level.

Table 16

ADJ Pin	EN Pin	Internal Circuit	$V_{OUT}$	Current Consumption
"H": ON	"H": ON	Operate	$\cong V_{ADJ}$	$I_{SS1}$
"H": ON	"L": OFF	Stop	$V_{SS}^{*1}$	$I_{SS2}$
"L": OFF	"H": ON	Stop	$V_{SS}^{*1}$	$I_{SS2}$
"L": OFF	"L": OFF	Stop	$V_{SS}^{*1}$	$I_{SS2}$

\*1. The VOUT pin is not pulled down internally. The VOUT pin voltage changes to  $V_{SS}$  level by the load connected to the VOUT pin.

#### 4. Overcurrent protection circuit

This IC includes an overcurrent protection circuit which having the characteristics shown in "1. Output voltage vs. Output current (When load current increases) (Ta = +25°C)" in "■ Characteristics (Typical Data)", in order to limit an excessive output current and overcurrent of the output transistor due to short-circuiting between the VOUT pin and the VSS pin.

When the load current increases and reaches the limit current ( $I_{LIM}$ ), the overcurrent protection circuit operates, and the output current is limited based on  $I_{LIM}$ . When the output is short-circuited (the VOUT pin is shorted to the VSS pin), the output current is limited to short-circuit current ( $I_{short}$ ).  $I_{LIM}$  and  $I_{short}$  are internally set at 500 mA typ.

This IC restarts the tracking operation over VOUT and VADJ when the output transistor is released from the overcurrent status.

**Caution** This overcurrent protection circuit does not work as for thermal protection. If this IC long keeps short circuiting inside, pay attention to the conditions of input voltage and load current so that, under the usage conditions including short circuit, the loss of the IC will not exceed power dissipation of the package.

#### 5. Thermal shutdown circuit

This IC has a built-in thermal shutdown circuit to limit overheating. When the junction temperature increases to 175°C typ., the thermal shutdown circuit becomes the detection status, and the tracking operation is stopped. When the junction temperature decreases to 165°C typ., the thermal shutdown circuit becomes the release status, and the tracking operation is restarted.

If the thermal shutdown circuit becomes the detection status due to self-heating, the tracking operation is stopped and  $V_{OUT}$  decreases. For this reason, the self-heating is limited and the temperature of the IC decreases. The thermal shutdown circuit becomes release status when the temperature of the IC decreases, and the tracking operation is restarted, thus the self-heating is generated again. Repeating this procedure makes the waveform of  $V_{OUT}$  into a pulse-like form. This phenomenon continues unless decreasing either or both of  $V_{IN}$  and  $I_{OUT}$  in order to reduce the internal power consumption, or decreasing the ambient temperature. Note that the product may suffer physical damage such as deterioration if the above phenomenon occurs continuously.

**Caution** If a large load current flows during the restart process of the tracking operation after the thermal shutdown circuit changes to the release status from the detection status, the thermal shutdown circuit becomes the detection status again due to self-heating, and a problem may happen in the restart of the tracking operation. A large load current, for example, occurs when charging to the  $C_L$  whose capacitance is large.

Perform thorough evaluation including the temperature characteristics with an actual application to select  $C_L$ .

Table 17

Thermal Shutdown Circuit	$V_{OUT}$
Release: 165°C typ.*1	$\cong V_{ADJ}$
Detection: 175°C typ.*1	$V_{SS}$ *2

\*1. Junction temperature

\*2. The VOUT pin is not pulled down internally.

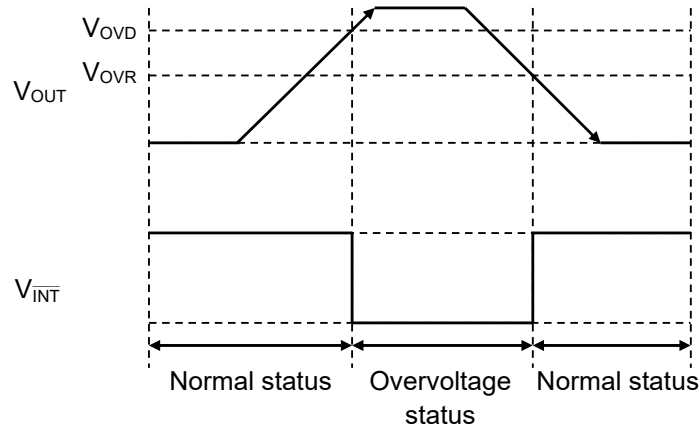
The VOUT pin voltage changes to  $V_{SS}$  level by the load connected to the VOUT pin.

**6. Overvoltage detection circuit**

A/B type of this IC has a built-in overvoltage detection circuit which monitors the output voltage ( $V_{OUT}$ ). This IC detects the overvoltage when  $V_{OUT} \geq V_{OVD}$ . When overvoltage is detected, The  $\overline{INT}$  pin outputs  $V_{SS}$  level.

**Table 18**

Overvoltage Detection Voltage ( $V_{OVD}$ )	Overvoltage Release Voltage ( $V_{OVR}$ )
$V_{ADJ} + 0.09$ V typ.	$V_{ADJ} + 0.08$ V typ.



**Figure 21**

**7. Anomaly notification Function**

Anomaly notification function monitors the IC status and outputs signal from the  $\overline{INT}$  pin of the Nch open-drain output. Pull-up level or  $V_{SS}$  level is output to  $\overline{INT}$  pin depending on the IC status as shown in **Table 19**. A delay time of 250  $\mu$ s typ. is set for the  $\overline{INT}$  pin pull-up. The  $\overline{INT}$  pin is pulled-up by an external resistor, but the voltage applied to the pin should not exceed the absolute maximum ratings.

**Table 19  $\overline{INT}$  Pin Output Voltage**

Product Type	Normal Status	Overvoltage Detection Status ( $V_{OUT} \geq V_{OVD}$ )	Ground Fault Detection Status ( $I_{OUT} \geq I_{LIMD}$ )	Thermal Shutdown Status ( $T_J \geq T_{SD}$ )
A	Pull-up level	$V_{SS}$	$V_{SS}$	$V_{SS}$
B	Pull-up level	$V_{SS}$	–	$V_{SS}$
C	Pull-up level	–	$V_{SS}$	$V_{SS}$

**Remark** During power-off ( $V_{ADJ} = "L"$  or  $V_{EN} = "L"$ ),  $\overline{INT}$  pin becomes pull-up level.



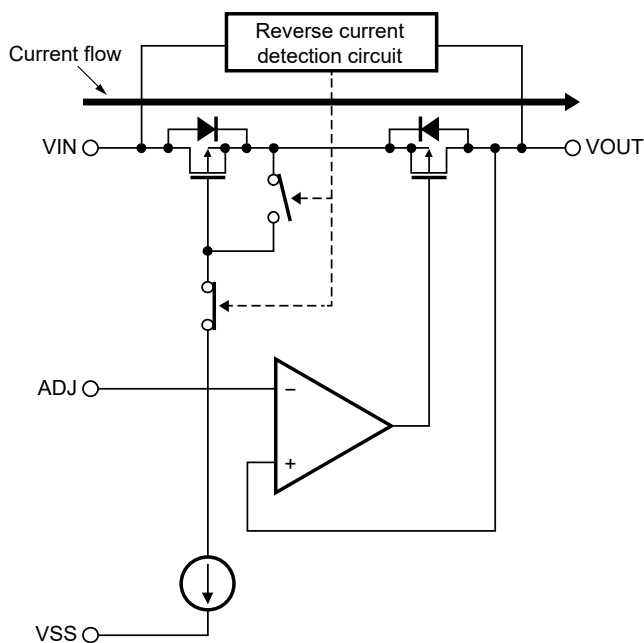
### 8. Reverse current protection function

The reverse current protection function compares values of  $V_{IN}$  and  $V_{OUT}$ , and prevents the current from flowing to the  $V_{IN}$  pin from the  $V_{OUT}$  pin.

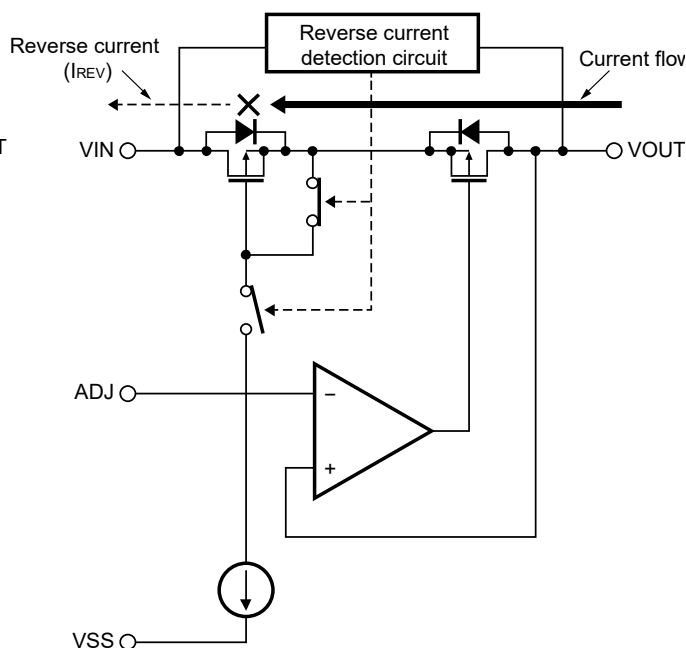
During the reverse current protection mode, the reverse current detection circuit turns off the reverse current protection transistor and blocks the reverse current from the  $V_{OUT}$  pin.

In the case of  $V_{OUT} - V_{IN} < V_{REVD}$ , this IC is in normal operation mode (refer to **Figure 22**). The reverse current protection mode is detected when  $V_{OUT} - V_{IN} \geq V_{REVD}$  (refer to **Figure 23**). In order to insure the stable operation, there is also a hysteresis for detection and release of the reverse current protection mode. Therefore, the reverse current protection mode is released when  $V_{OUT} - V_{IN} \leq V_{REVR}$ .

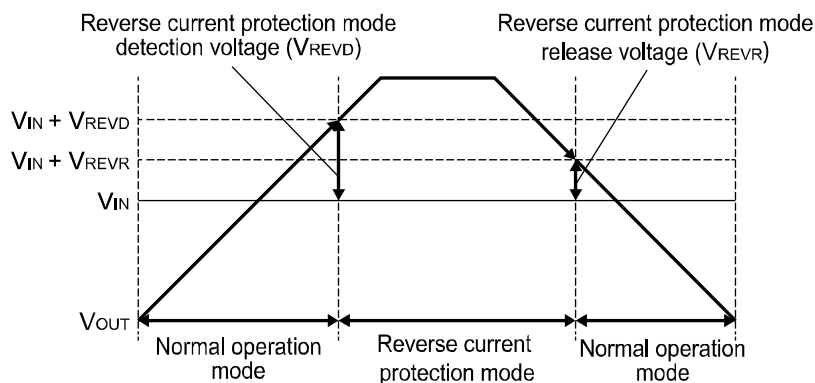
The reverse current protection function also operates when the ADJ pin or EN pin is set to OFF level.



**Figure 22 Normal Operation Mode**



**Figure 23 Reverse Current Protection Mode**



**Figure 24**

**Table 20**

Reverse current protection mode detection voltage ( $V_{REVD}$ )	Reverse current protection mode release voltage ( $V_{REVR}$ )
0.50 V typ.	0.33 V typ.

## ■ Precautions

- Generally, when a voltage tracker is used under the condition that the load current value is small (0.1 mA or less), the output voltage may increase due to the leakage current of an output transistor.
- Generally, when a voltage tracker is used under the condition that the temperature is high, the output voltage may increase due to the leakage current of an output transistor.
- Generally, when the ADJ pin and EN pin of a voltage tracker is used under the condition of OFF, the output voltage may increase due to the leakage current of an output transistor.
- Generally, when a voltage tracker is used under the condition that the impedance of the power supply is high, an oscillation may occur. Perform thorough evaluation including the temperature characteristics with an actual application to select  $C_{IN}$ .
- Generally, in a voltage tracker, an oscillation may occur depending on the selection of the external parts. The following use conditions are recommended in this IC, however, perform thorough evaluation including the temperature characteristics with an actual application to select  $C_{IN}$  and  $C_L$ .

Input capacitor ( $C_{IN}$ ): A ceramic capacitor with capacitance of 4.7  $\mu$ F or more is recommended.

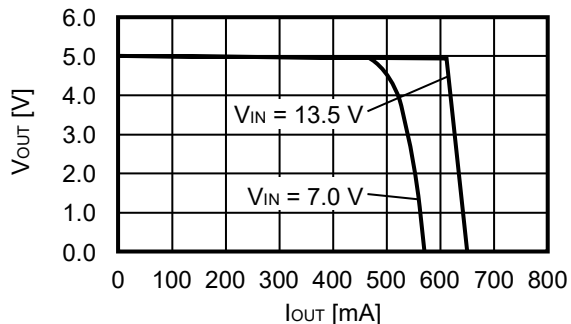
Output capacitor ( $C_L$ ): A ceramic capacitor with capacitance of 4.7  $\mu$ F to 1000  $\mu$ F is recommended.

- Generally, in a voltage tracker, the values of an overshoot and an undershoot in the output voltage vary depending on the variation factors of input voltage start-up, input voltage fluctuation and load fluctuation etc., or the capacitance of  $C_{IN}$  or  $C_L$  and the value of the equivalent series resistance (ESR), which may cause a problem to the stable operation. Perform thorough evaluation including the temperature characteristics with an actual application to select  $C_{IN}$  and  $C_L$ .
- Generally, in a voltage tracker, an overshoot may occur in the output voltage momentarily if the input voltage steeply changes when the input voltage is started up or the input voltage fluctuates etc. Perform thorough evaluation including the temperature characteristics with an actual application to confirm no problems happen.
- Generally, in a voltage tracker, if the VOUT pin is steeply shorted with GND, a negative voltage exceeding the absolute maximum ratings may occur in the VOUT pin due to resonance phenomenon of the inductance and the capacitance including  $C_L$  on the application. The resonance phenomenon is expected to be weakened by inserting a series resistor into the resonance path, and the negative voltage is expected to be limited by inserting a protection diode between the VOUT pin and the VSS pin.
- If the input voltage is started up steeply under the condition that the capacitance of  $C_L$  is large, the thermal shutdown circuit may be in the detection status by self-heating due to the charge current to  $C_L$ .
- Make sure of the conditions for the input voltage, output voltage and the load current so that the internal loss does not exceed the power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- When considering the output current value that this IC is able to output, make sure of the output current value specified in **Table 14** in "■ Recommended Operation Conditions" and footnote \*1 of the table.
- Wiring patterns on the application related to the VIN pin, the VOUT pin and the VSS pin should be designed so that the impedance is low. When mounting  $C_{IN}$  between the VIN pin and the VSS pin and  $C_L$  between the VOUT pin and the VSS pin, connect the capacitors as close as possible to the respective destination pins of this IC.
- In the package equipped with heat sink of backside, mount the heat sink firmly. Since the heat radiation differs according to the condition of the application, perform thorough evaluation with an actual application to confirm no problems happen.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

## ■ Characteristics (Typical Data)

### 1. Output voltage vs. Output current (When load current increases) (Ta = +25°C)

#### 1.1 V<sub>ADJ</sub> = 5.0 V

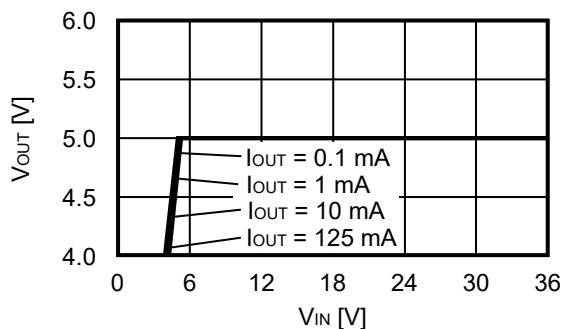


**Remark** In determining the output current, attention should be paid to the following.

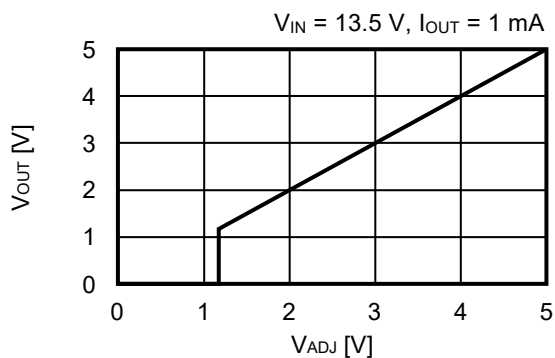
1. The output current value and footnote \*1 of Table 14 in "■ Recommended Operation Conditions"
2. Power dissipation

### 2. Output voltage vs. Input voltage (Ta = +25°C)

#### 2.1 V<sub>ADJ</sub> = 5.0 V

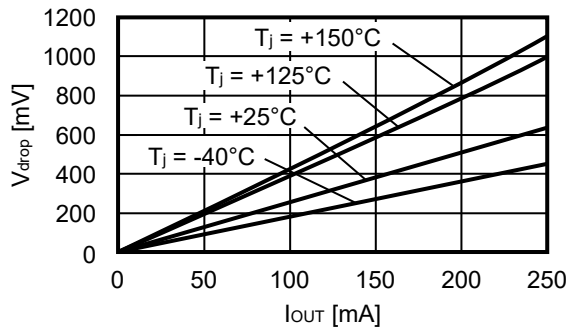


### 3. Output voltage vs. ADJ pin input voltage (Ta = +25°C)



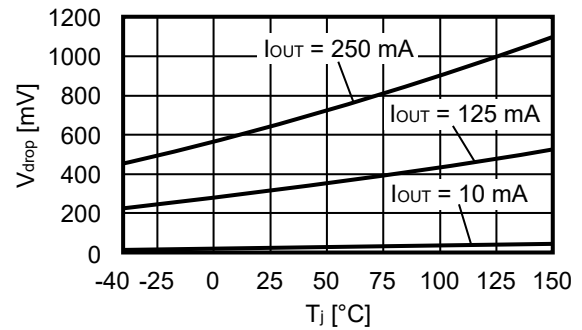
**4. Dropout voltage vs. Output current**

4.1  $V_{ADJ} = 5.0\text{ V}$

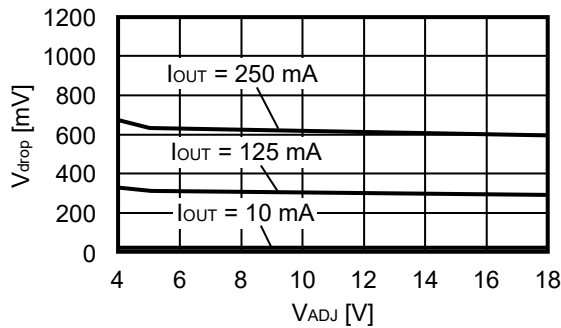


**5. Dropout voltage vs. Junction temperature**

5.1  $V_{ADJ} = 5.0\text{ V}$

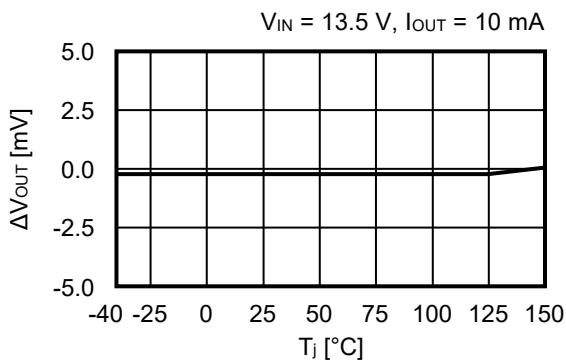


**6. Dropout voltage vs. Set output voltage ( $T_a = +25^\circ\text{C}$ )**



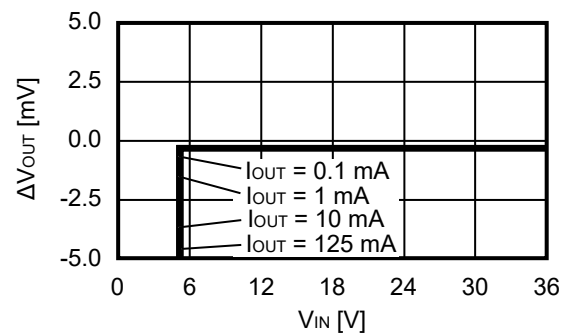
**7. Offset voltage vs. Junction temperature**

7.1  $V_{ADJ} = 5.0\text{ V}$



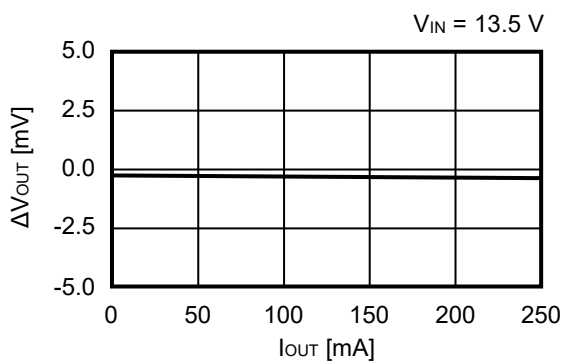
**8. Offset voltage vs. Input voltage ( $T_a = +25^\circ\text{C}$ )**

8.1  $V_{ADJ} = 5.0\text{ V}$



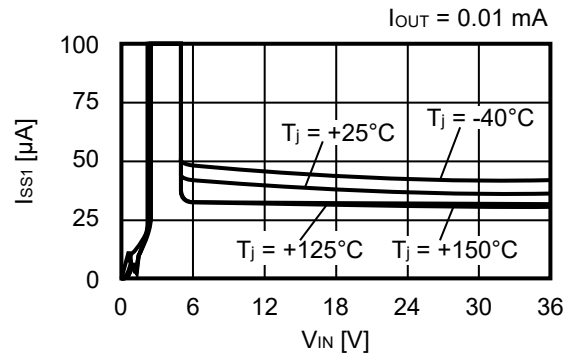
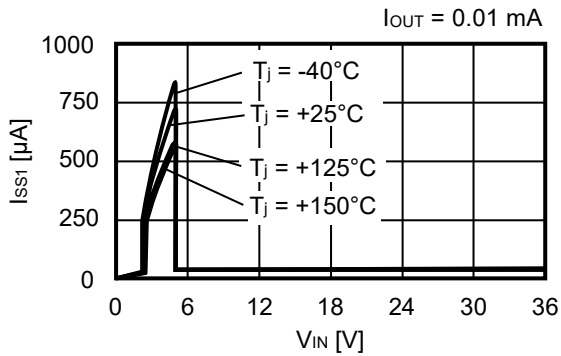
**9. Offset voltage vs. Output current ( $T_a = +25^\circ\text{C}$ )**

9.1  $V_{ADJ} = 5.0\text{ V}$

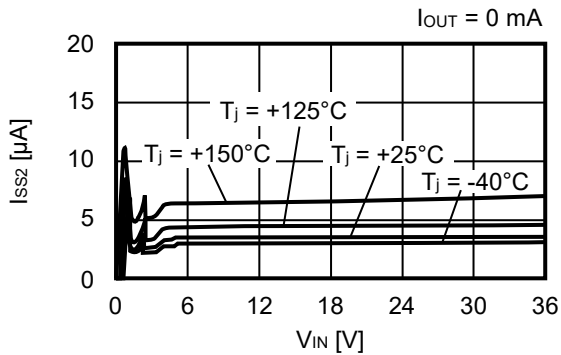


### 10. Current consumption vs. Input voltage

#### 10.1 $V_{ADJ} = 5.0$ V (during operation)

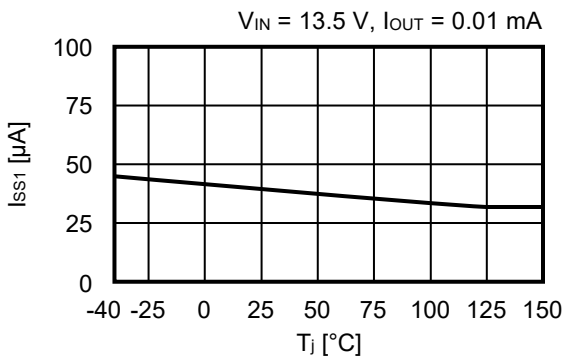


#### 10.2 $V_{ADJ} = 0.0$ V (Power-off)

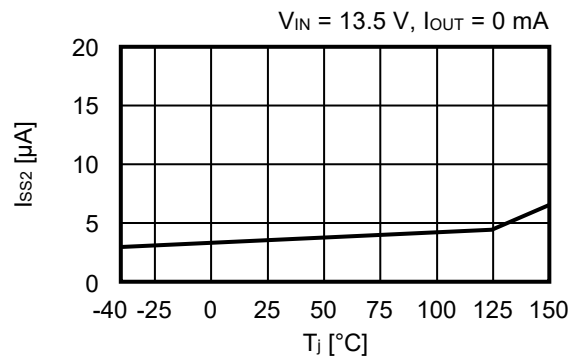


### 11. Current consumption vs. Junction temperature

#### 11.1 $V_{ADJ} = 5.0$ V (during operation)

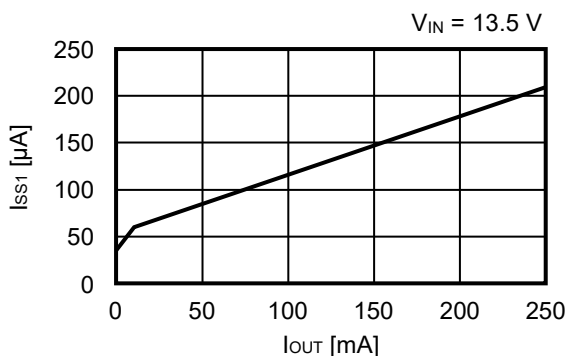


#### 11.2 $V_{ADJ} = 0.0$ V (Power-off)



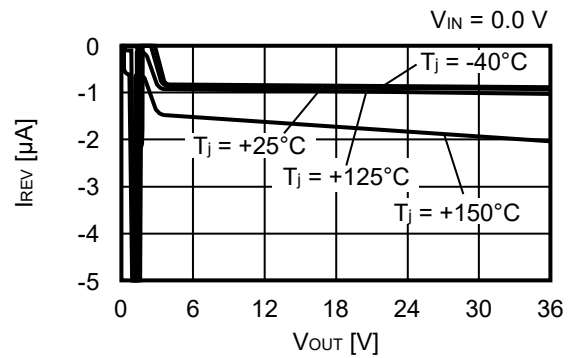
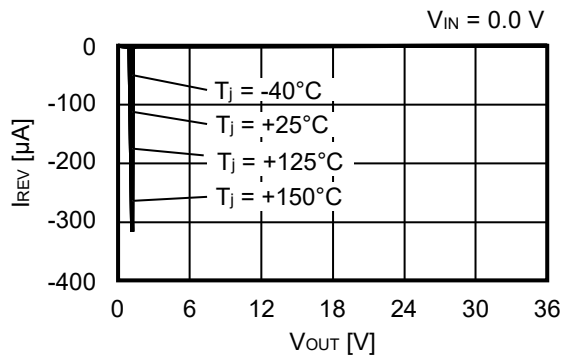
### 12. Current consumption vs. Output current ( $T_a = +25^\circ C$ )

#### 12.1 $V_{ADJ} = 5.0$ V

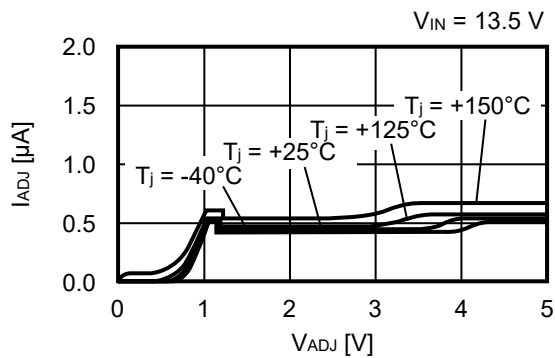


**13. Reverse current vs. VOUT pin voltage**

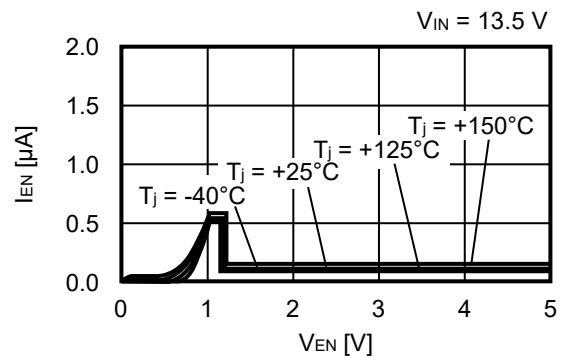
13.1 V<sub>ADJ</sub> = 5.0 V



**14. ADJ pin current vs. ADJ pin voltage**

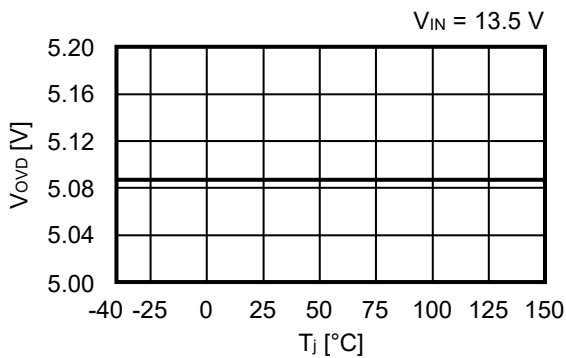


**15. EN pin current vs. EN pin voltage**

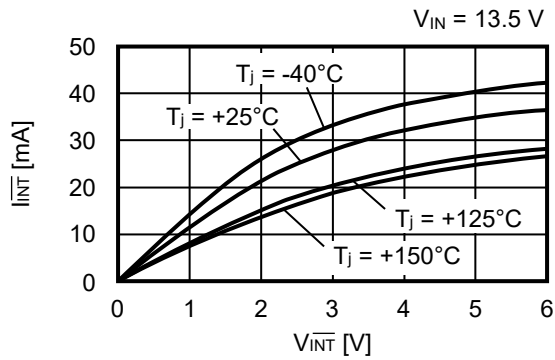


**16. Overvoltage detection voltage vs. Junction temperature**

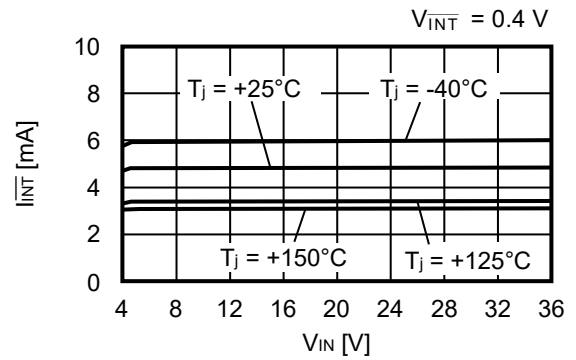
16.1 V<sub>ADJ</sub> = 5.0 V



17.  $\overline{INT}$  pin output current vs.  $\overline{INT}$  pin voltage

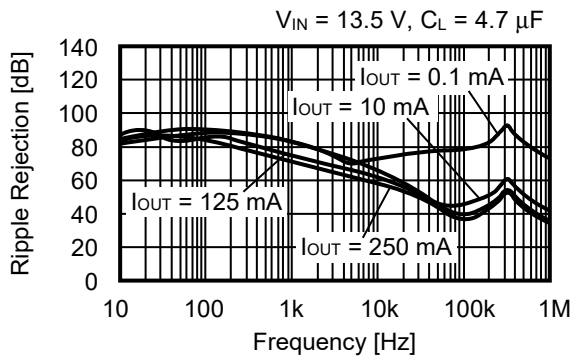


18.  $\overline{INT}$  pin output current vs. Input voltage



19. Ripple rejection ( $T_a = +25^\circ\text{C}$ )

19.1  $V_{ADJ} = 5.0\text{ V}$

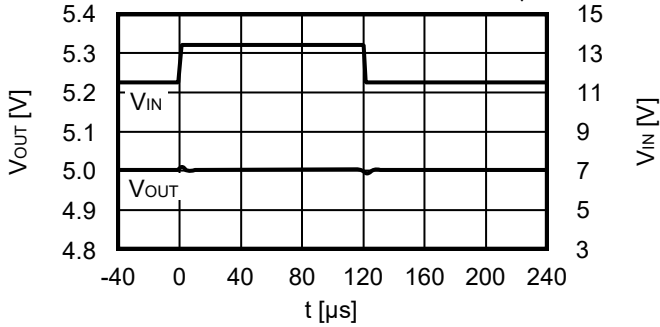


■ Reference Data

1. Characteristics of input transient response (Ta = +25°C)

1.1 V<sub>ADJ</sub> = 5.0 V

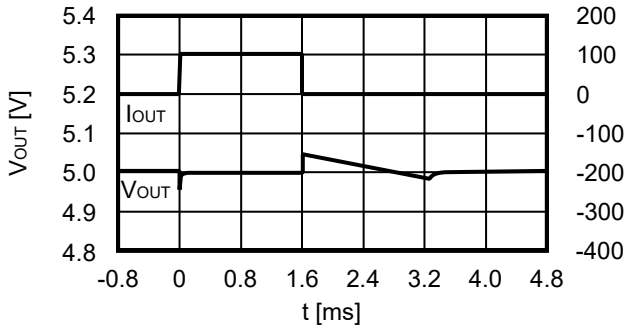
I<sub>OUT</sub> = 100 mA, C<sub>L</sub> = 4.7 μF,  
 V<sub>IN</sub> = 11.5 V ↔ 13.5 V, t<sub>r</sub> = t<sub>f</sub> = 2.0 μs



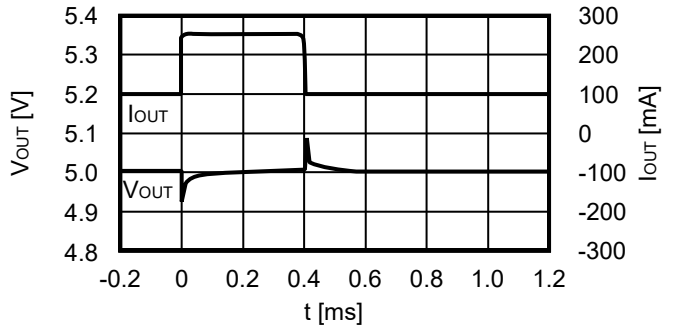
2. Characteristics of load transient response (Ta = +25°C)

2.1 V<sub>ADJ</sub> = 5.0 V

V<sub>IN</sub> = 13.5 V, C<sub>IN</sub> = C<sub>L</sub> = 4.7 μF,  
 I<sub>OUT</sub> = 1 mA ↔ 100 mA



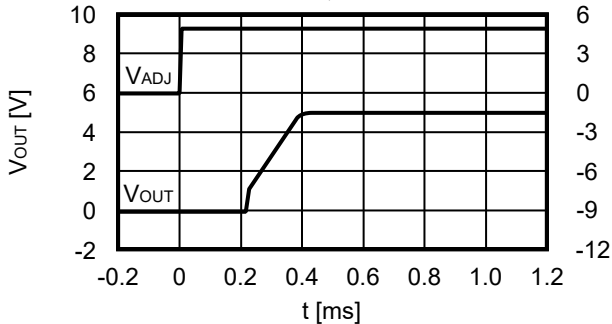
V<sub>IN</sub> = 13.5 V, C<sub>IN</sub> = C<sub>L</sub> = 4.7 μF,  
 I<sub>OUT</sub> = 100 mA ↔ 250 mA



3. Transient response characteristics of ADJ pin (Ta = +25°C)

3.1 V<sub>ADJ</sub> = 5.0 V

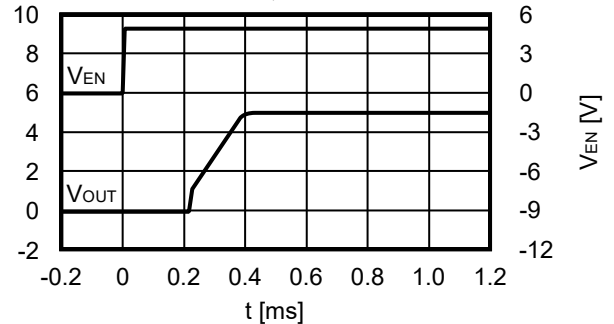
V<sub>IN</sub> = 13.5 V, C<sub>IN</sub> = C<sub>L</sub> = 4.7 μF,  
 I<sub>OUT</sub> = 100 mA, V<sub>ADJ</sub> = 0 V → 5.0 V



4. Transient response characteristics of EN pin (Ta = +25°C)

4.1 V<sub>ADJ</sub> = 5.0 V

V<sub>IN</sub> = 13.5 V, C<sub>IN</sub> = C<sub>L</sub> = 4.7 μF,  
 I<sub>OUT</sub> = 100 mA, V<sub>EN</sub> = 0 V → 5.0 V

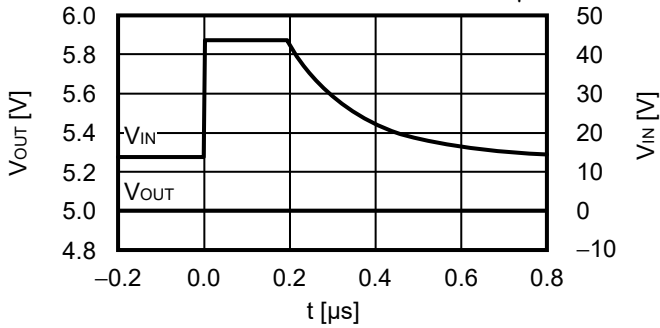




**5. Load dump characteristics (Ta = +25°C)**

**5.1 V<sub>ADJ</sub> = 5.0 V**

I<sub>OUT</sub> = 0.1 mA, V<sub>IN</sub> = 14.0 V ↔ 45.0 V,  
 C<sub>IN</sub> = C<sub>L</sub> = 4.7 μF



**6. Example of equivalent series resistance vs. Output current characteristics (Ta = -40°C to +125°C)**

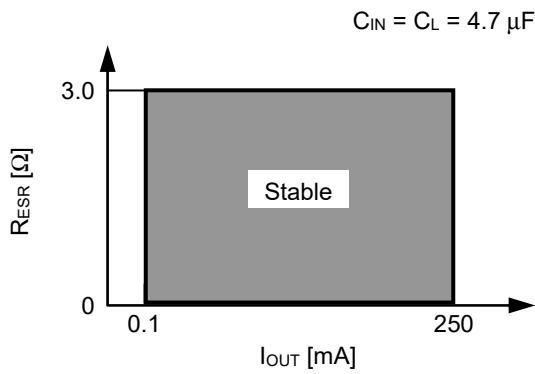
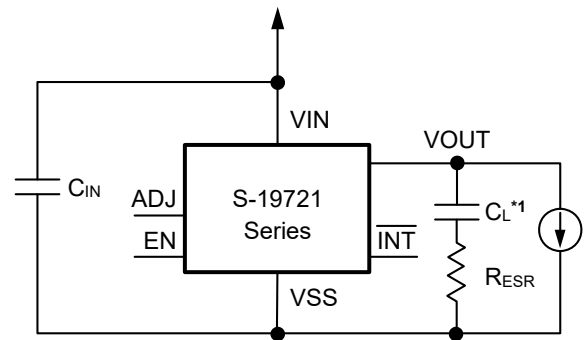


Figure 25

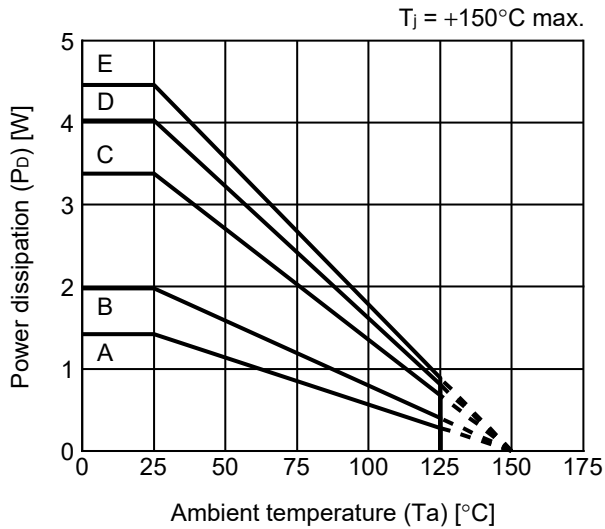


\*1. C<sub>L</sub>: TDK Corporation CGA6M1X8L1H475K (4.7  $\mu\text{F}$ )

Figure 26

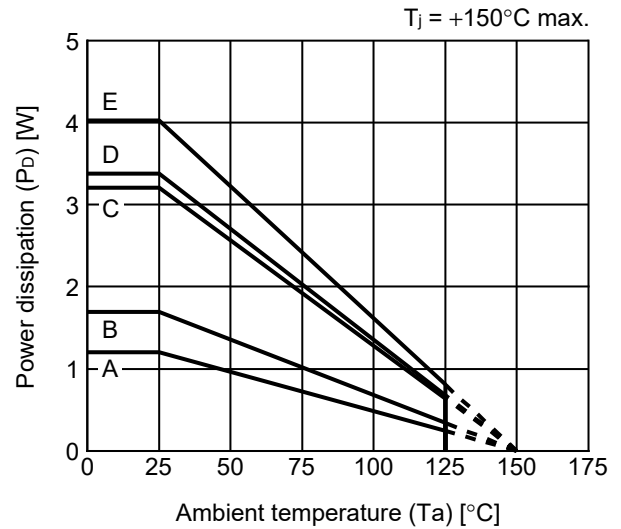
■ Power Dissipation

TO-252-9S



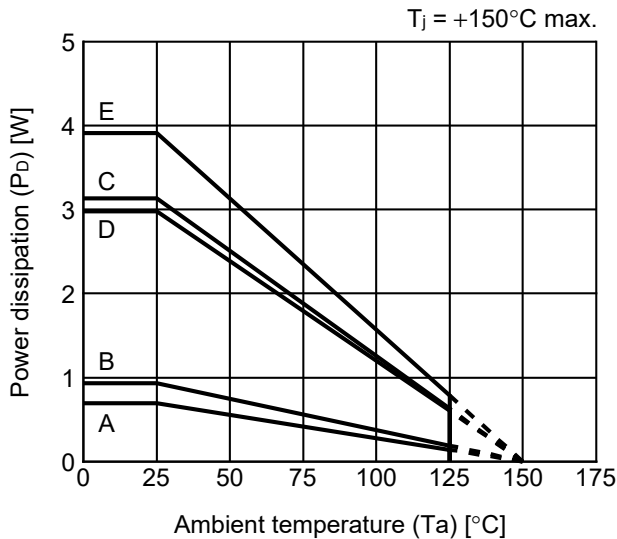
Board	Power Dissipation ( $P_D$ )
A	1.42 W
B	1.98 W
C	3.38 W
D	4.03 W
E	4.46 W

HSOP-8A



Board	Power Dissipation ( $P_D$ )
A	1.20 W
B	1.69 W
C	3.21 W
D	3.38 W
E	4.03 W

HSNT-8(2030)

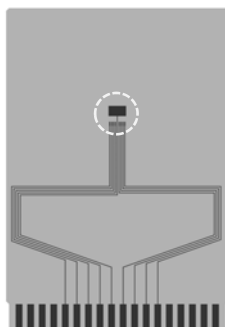


Board	Power Dissipation ( $P_D$ )
A	0.69 W
B	0.93 W
C	3.13 W
D	2.98 W
E	3.91 W

# TO-252-9S Test Board

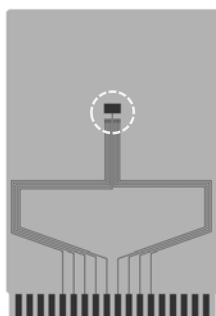
(1) Board A

 IC Mount Area



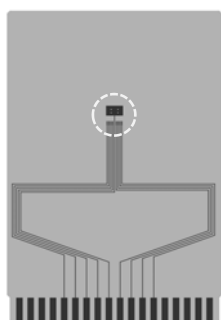
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



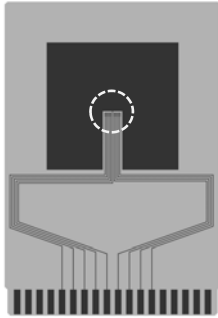
enlarged view

No. TO252-9S-A-Board-SD-1.0

# TO-252-9S Test Board

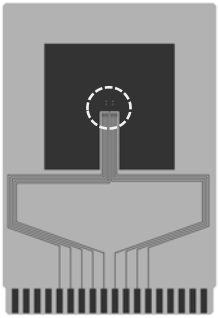
**(4) Board D**

 IC Mount Area



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm <sup>2</sup> t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

**(5) Board E**



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm <sup>2</sup> t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



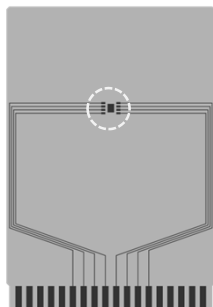
enlarged view

No. TO252-9S-A-Board-SD-1.0

# HSOP-8A Test Board

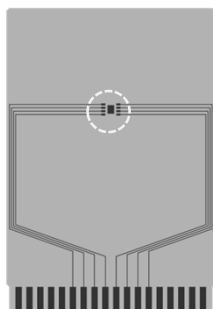
(1) Board A

 IC Mount Area



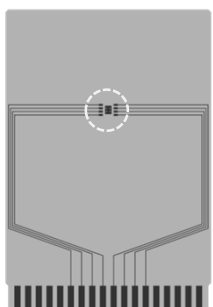
Item	Specification	
Size [mm]	114.3 x 76.2 x t1.6	
Material	FR-4	
Number of copper foil layer	2	
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via	-	

(2) Board B

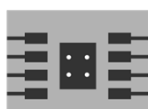


Item	Specification	
Size [mm]	114.3 x 76.2 x t1.6	
Material	FR-4	
Number of copper foil layer	4	
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via	-	

(3) Board C



Item	Specification	
Size [mm]	114.3 x 76.2 x t1.6	
Material	FR-4	
Number of copper foil layer	4	
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via	Number: 4 Diameter: 0.3 mm	



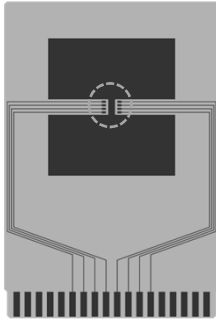
enlarged view

No. HSOP8A-A-Board-SD-1.0

# HSOP-8A Test Board

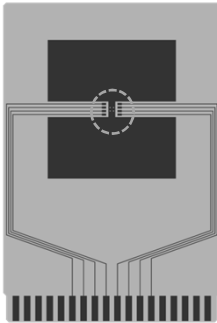
**(4) Board D**

 IC Mount Area



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm <sup>2</sup> t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

**(5) Board E**




Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm <sup>2</sup> t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



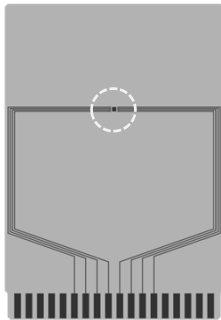
enlarged view

No. HSOP8A-A-Board-SD-1.0

# HSNT-8(2030) Test Board

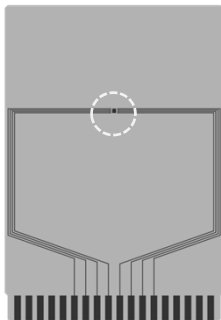
 IC Mount Area

(1) Board A



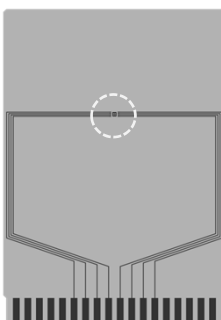
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C




Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



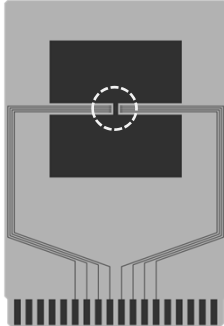
enlarged view

No. HSNT8-A-Board-SD-2.0

# HSNT-8(2030) Test Board

 IC Mount Area

## (4) Board D

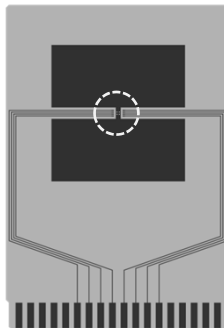


Item	Specification	
Size [mm]	114.3 x 76.2 x t1.6	
Material	FR-4	
Number of copper foil layer	4	
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm <sup>2</sup> t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via	-	



enlarged view

## (5) Board E



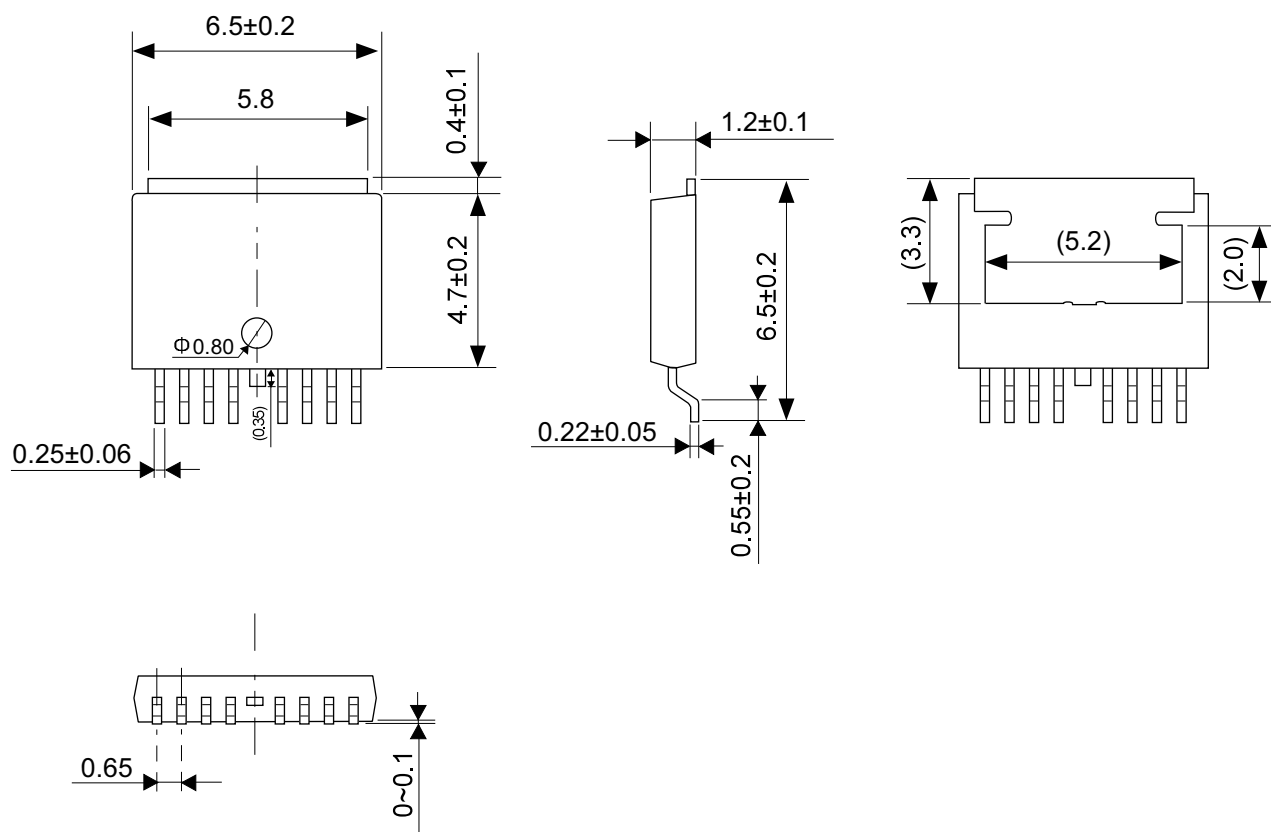
Item	Specification	
Size [mm]	114.3 x 76.2 x t1.6	
Material	FR-4	
Number of copper foil layer	4	
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm <sup>2</sup> t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via	Number: 4 Diameter: 0.3 mm	



enlarged view

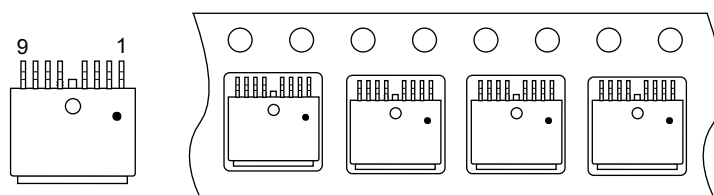
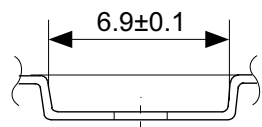
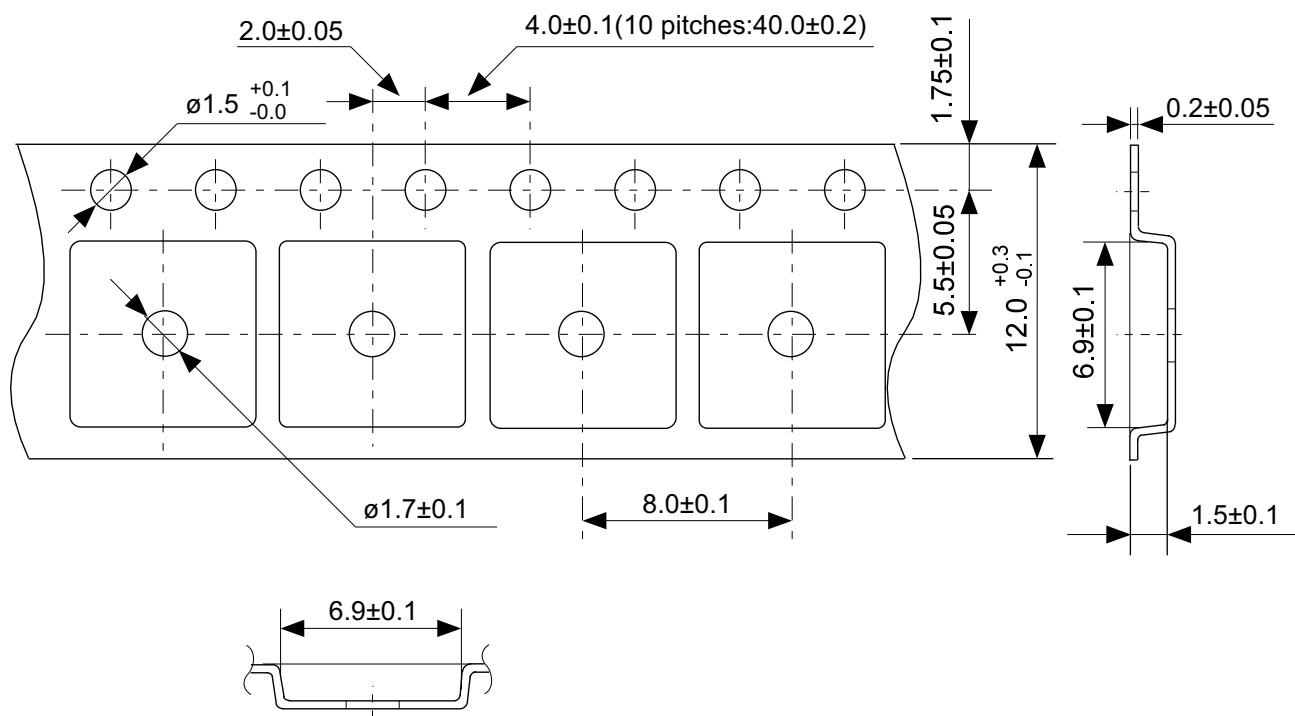
No. HSNT8-A-Board-SD-2.0





No. VA009-A-P-SD-2.0

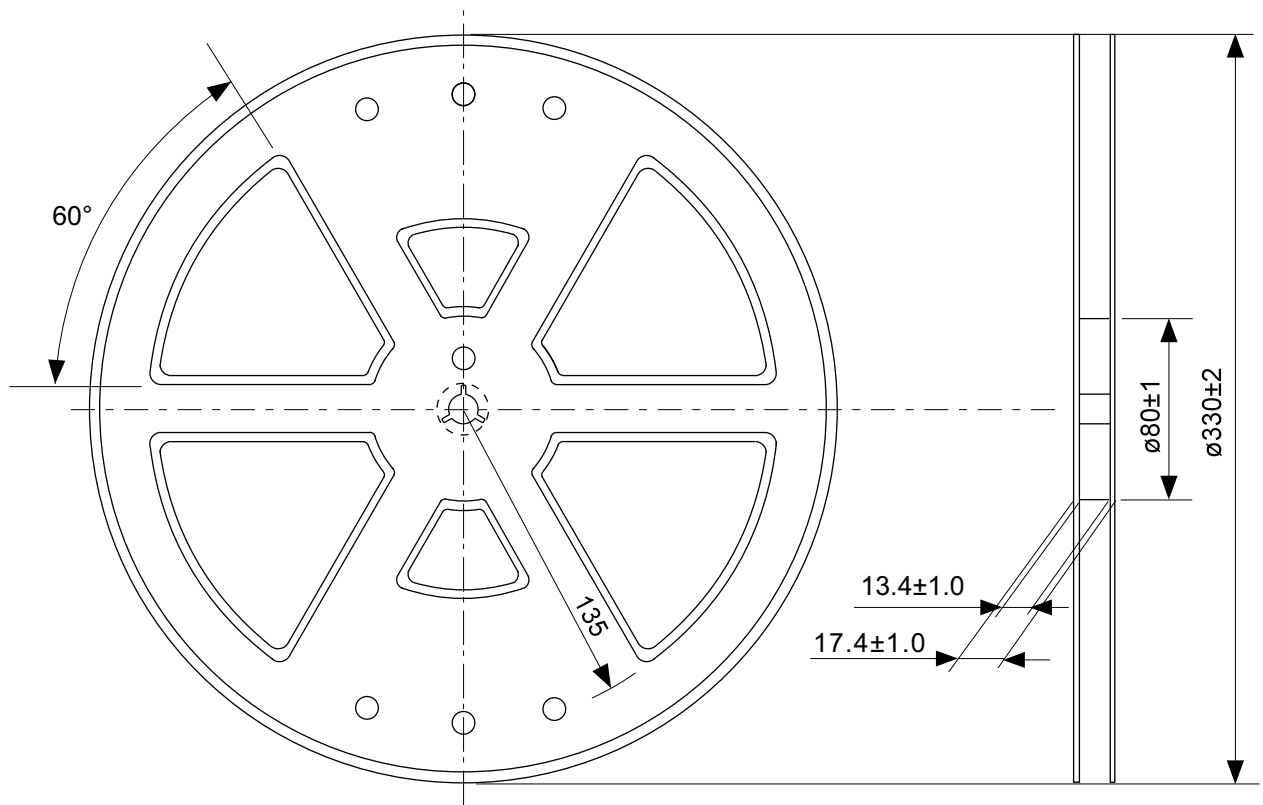
TITLE	TO252-9S-A-PKG Dimensions
No.	VA009-A-P-SD-2.0
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	



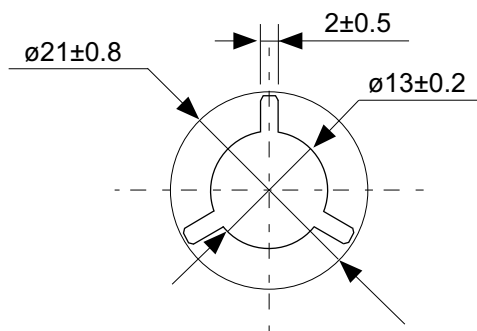
Feed direction →

No. VA009-A-C-SD-1.0

TITLE	TO252-9S-A-Carrier Tape
No.	VA009-A-C-SD-1.0
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	

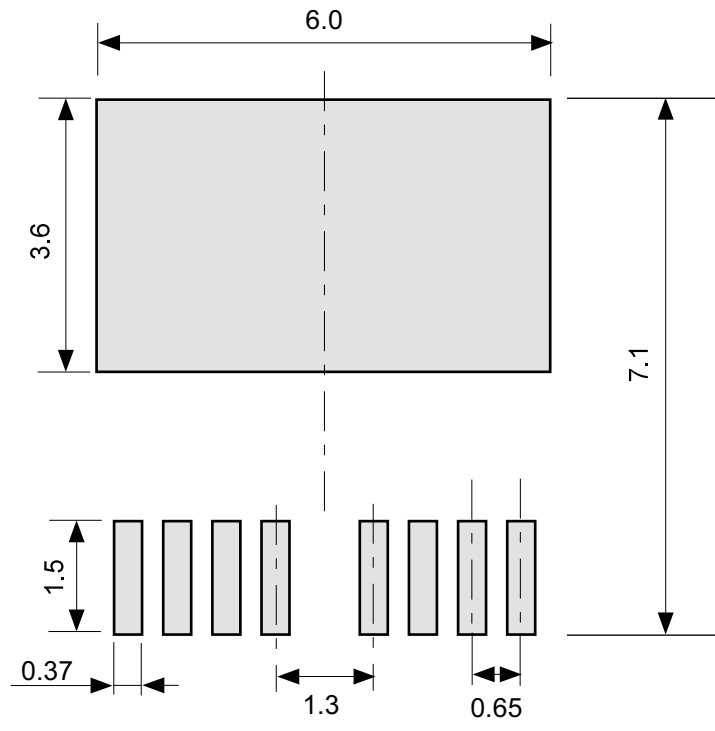


Enlarged drawing in the central part



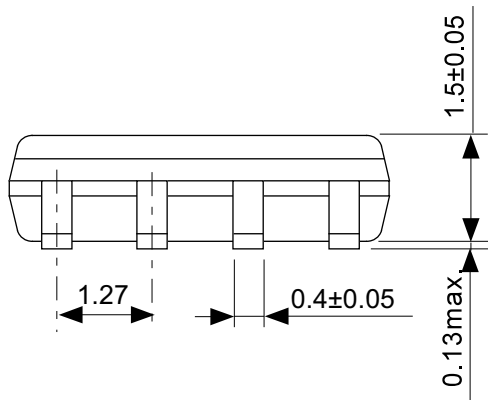
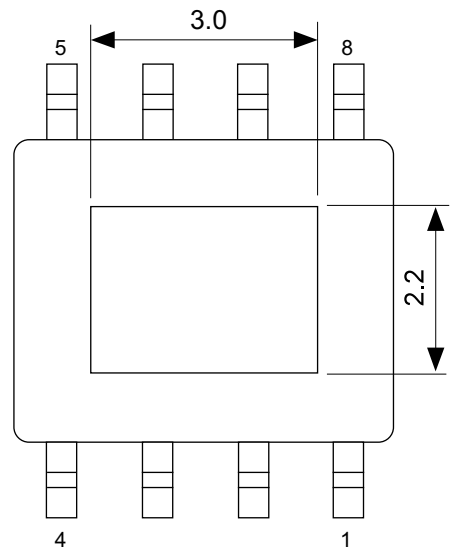
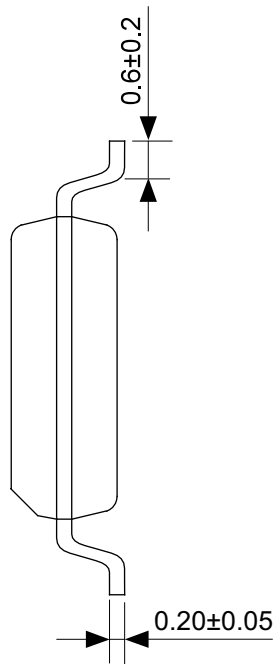
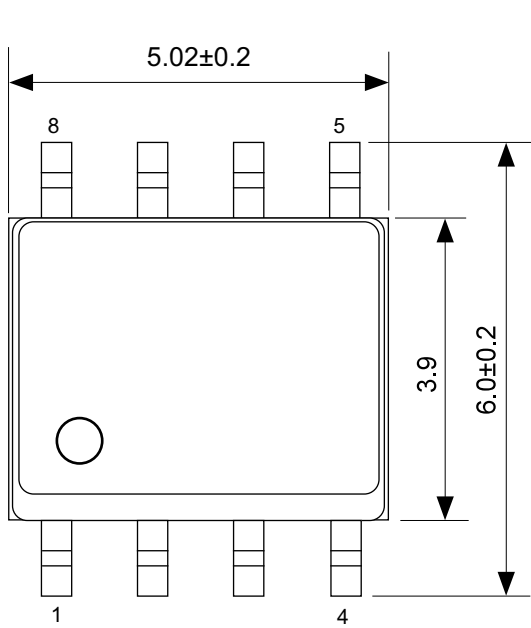
No. VA009-A-R-SD-1.1

TITLE	TO252-9S-A-Reel		
No.	VA009-A-R-SD-1.1		
ANGLE		QTY.	4,000
UNIT	mm		
<b>ABLIC Inc.</b>			



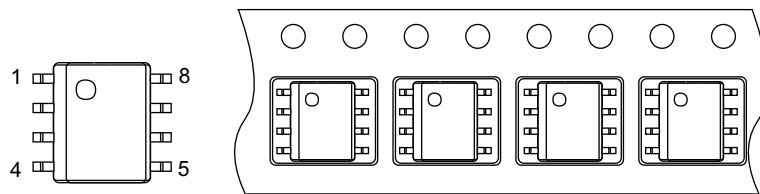
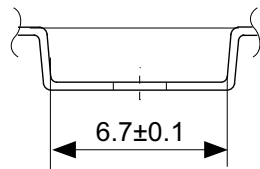
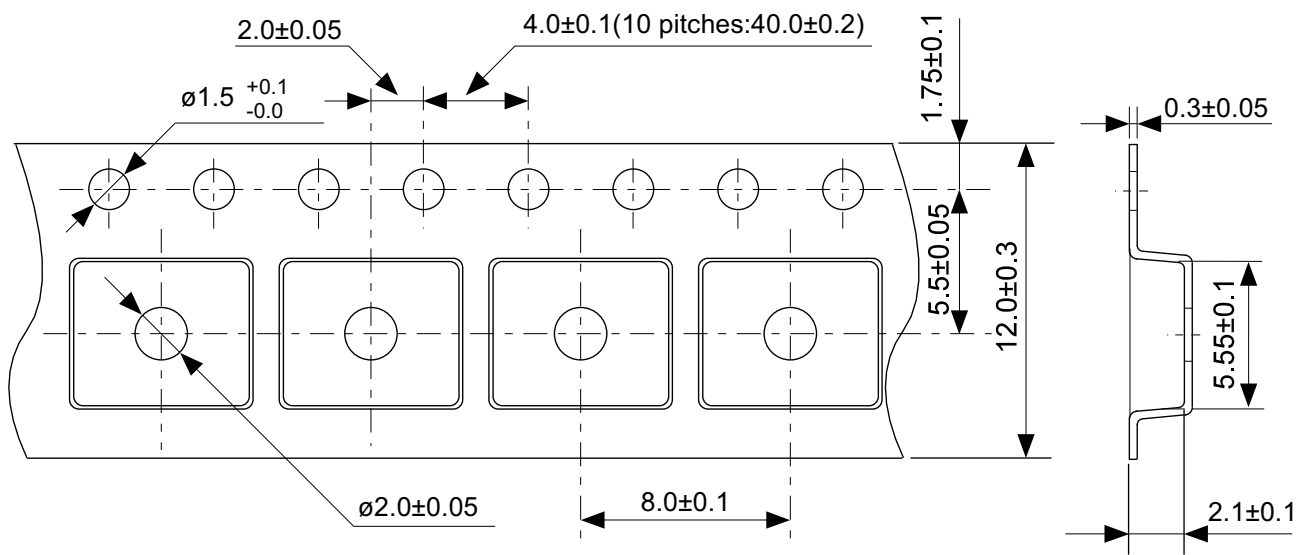
No. VA009-A-L-SD-1.0

TITLE	TO252-9S-A -Land Recommendation
No.	VA009-A-L-SD-1.0
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	



No. FH008-A-P-SD-2.0

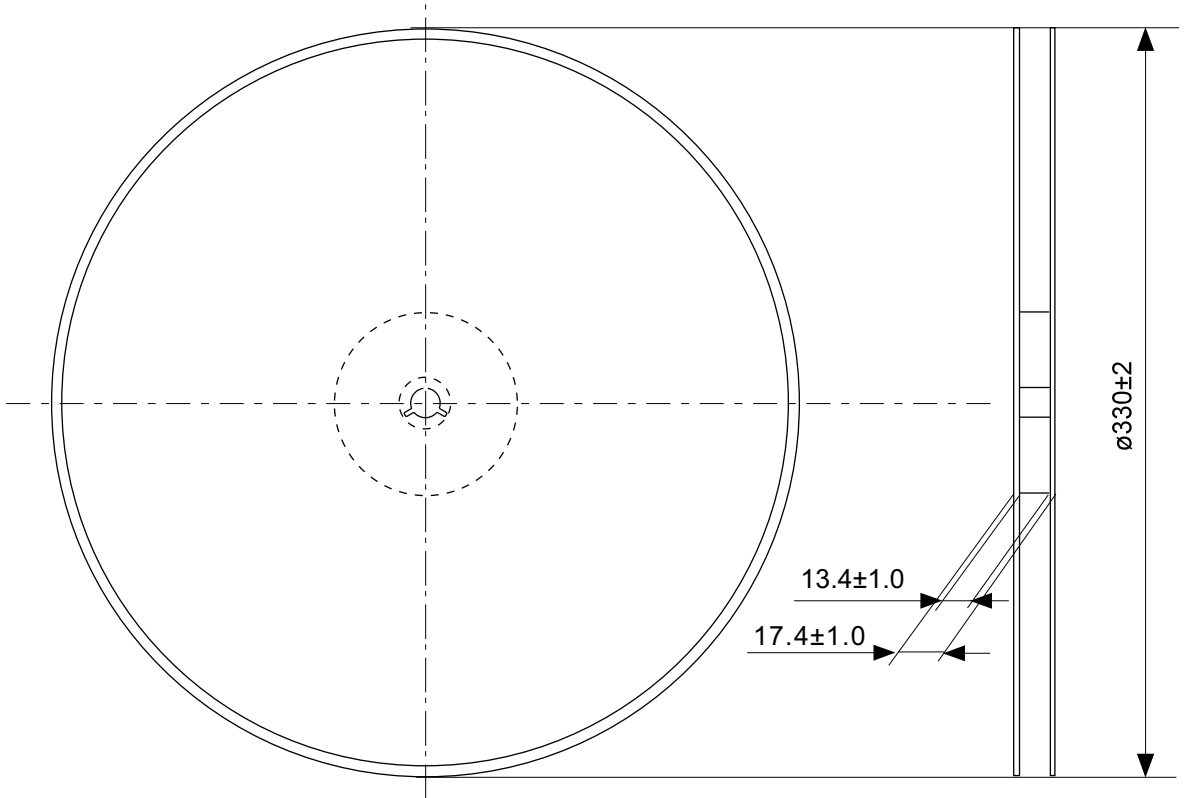
TITLE	HSOP8A-A-PKG Dimensions
No.	FH008-A-P-SD-2.0
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	



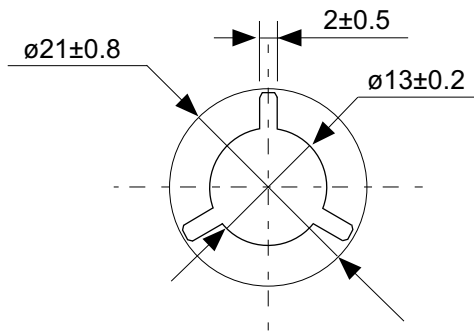
→  
Feed direction

No. FH008-A-C-SD-1.0

TITLE	HSOP8A-A-Carrier Tape
No.	FH008-A-C-SD-1.0
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	

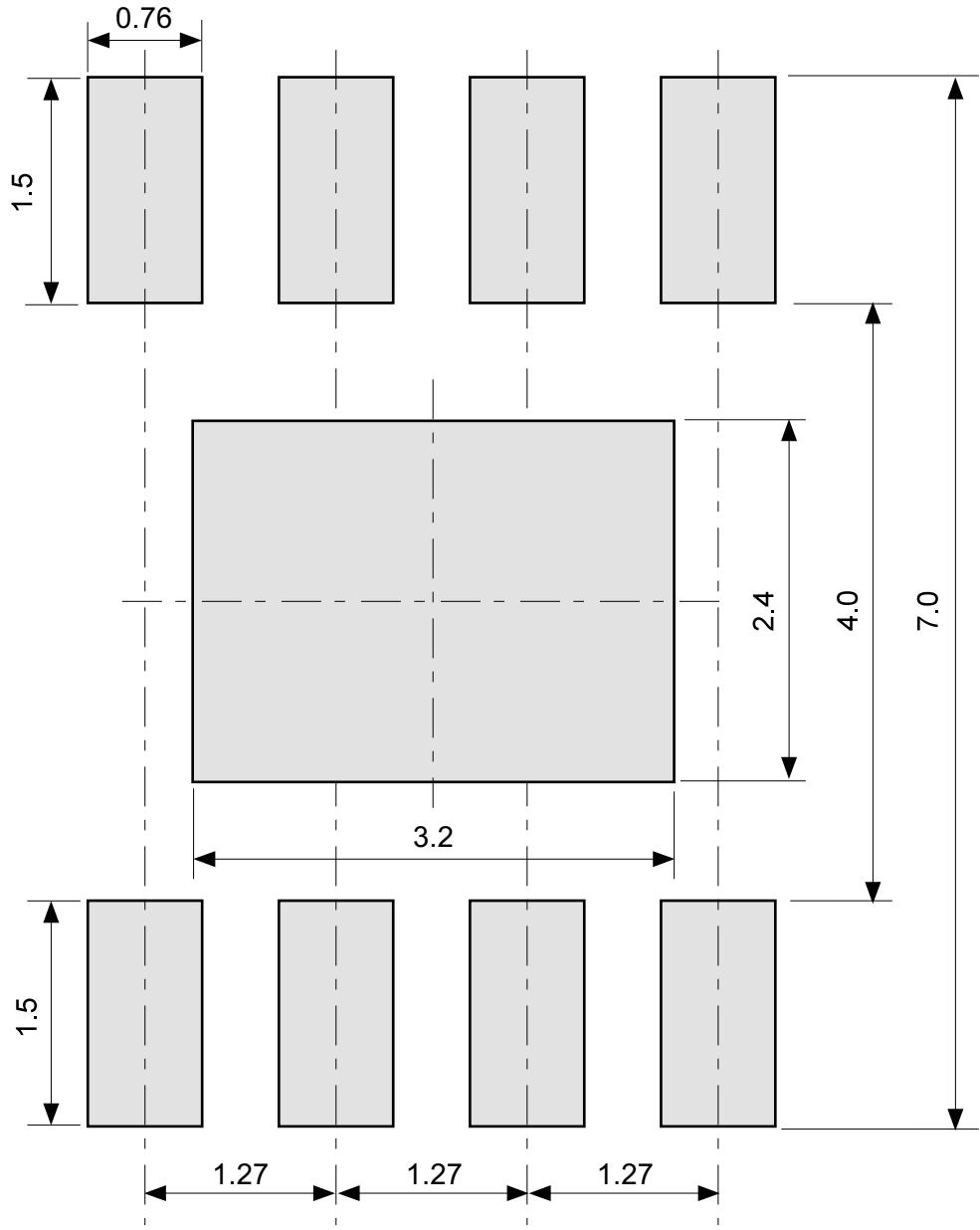


Enlarged drawing in the central part



No. FH008-A-R-SD-1.1

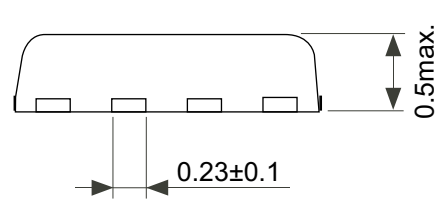
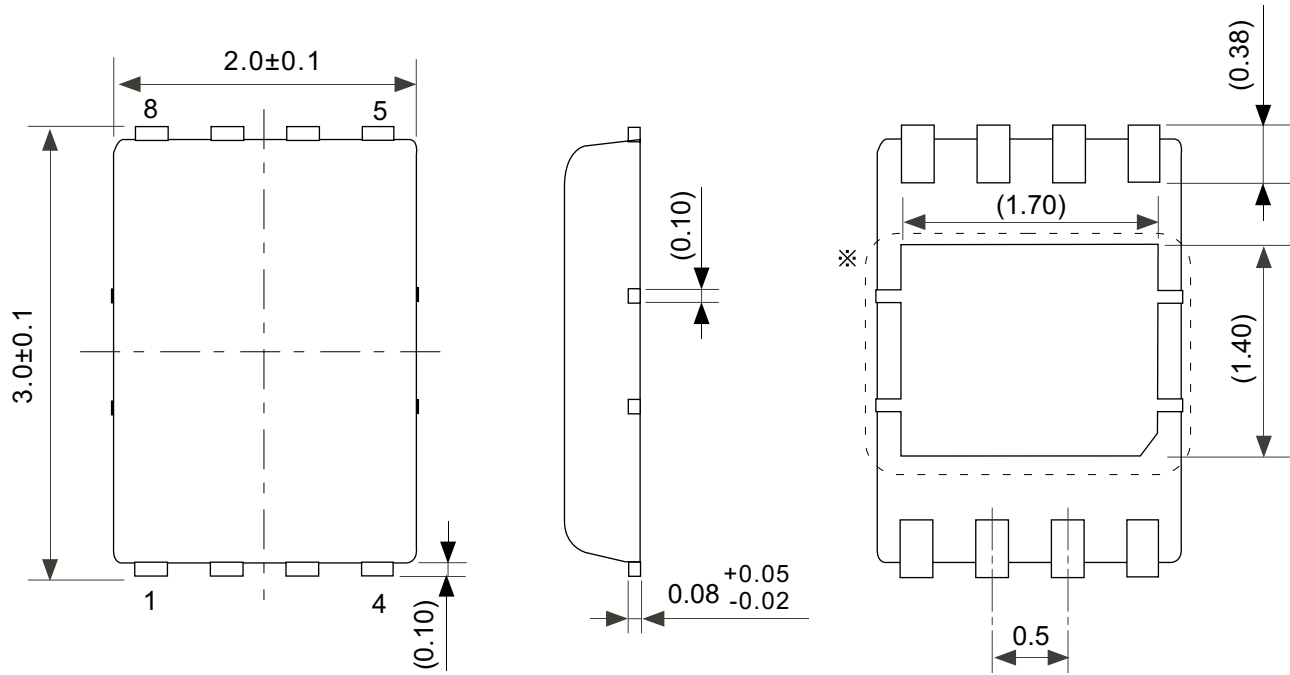
TITLE	HSOP8A-A-Reel		
No.	FH008-A-R-SD-1.1		
ANGLE		QTY.	4,000
UNIT	mm		
<b>ABLIC Inc.</b>			



No. FH008-A-L-SD-1.0

TITLE	HSOP8A-A -Land Recommendation
No.	FH008-A-L-SD-1.0
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	

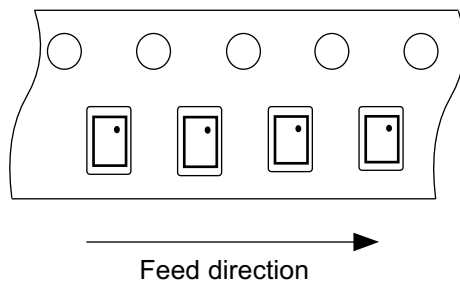
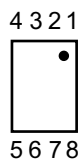
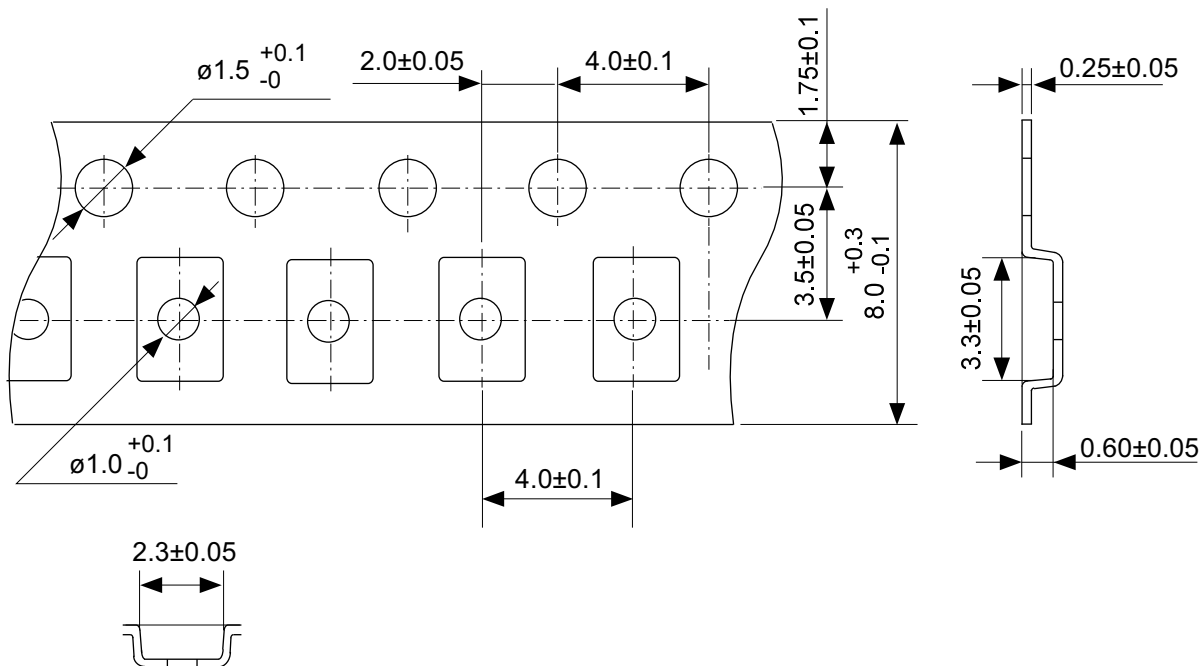




※ The heat sink of back side has different electric potential depending on the product.  
 Confirm specifications of each product.  
 Do not use it as the function of electrode.

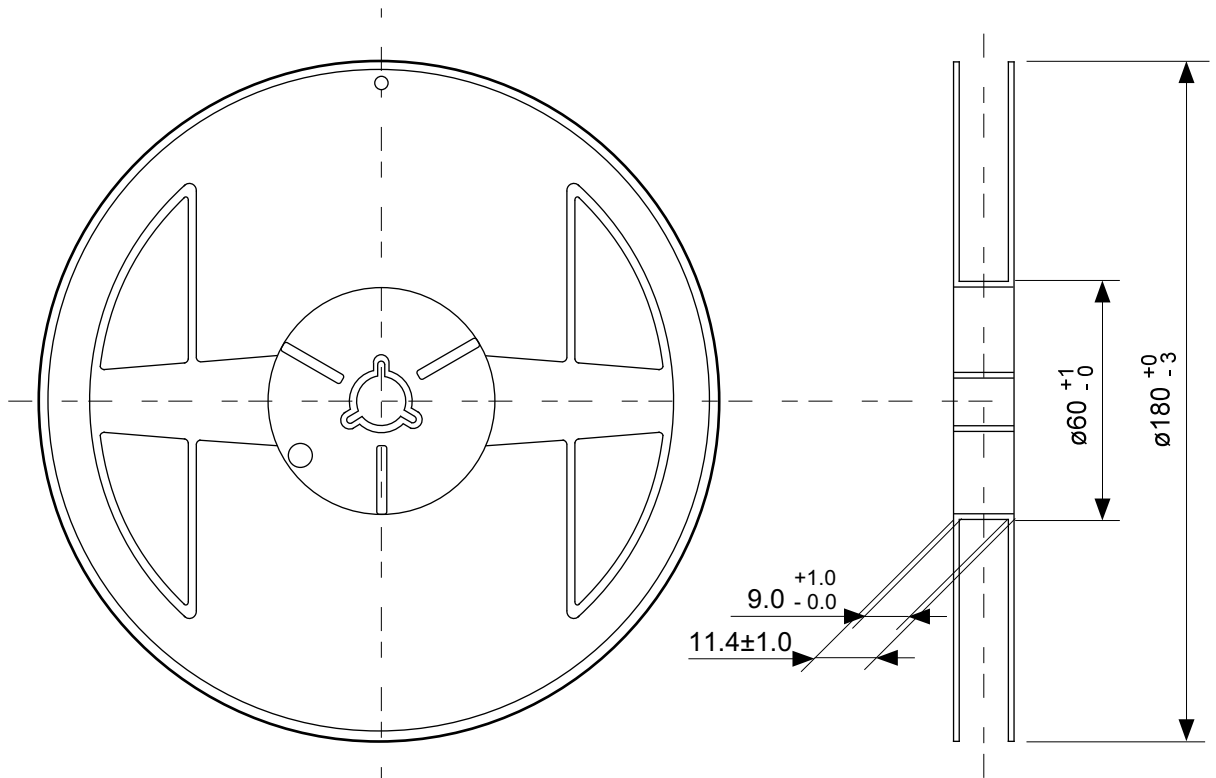
No. PP008-A-P-SD-2.0

TITLE	HSNT-8-A-PKG Dimensions
No.	PP008-A-P-SD-2.0
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	

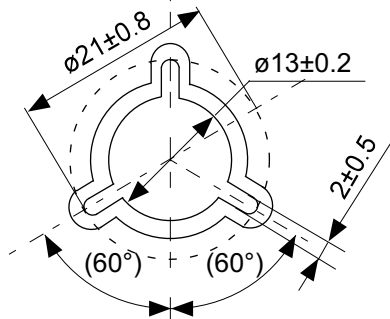


No. PP008-A-C-SD-1.0

TITLE	HSNT-8-A-Carrier Tape
No.	PP008-A-C-SD-1.0
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	

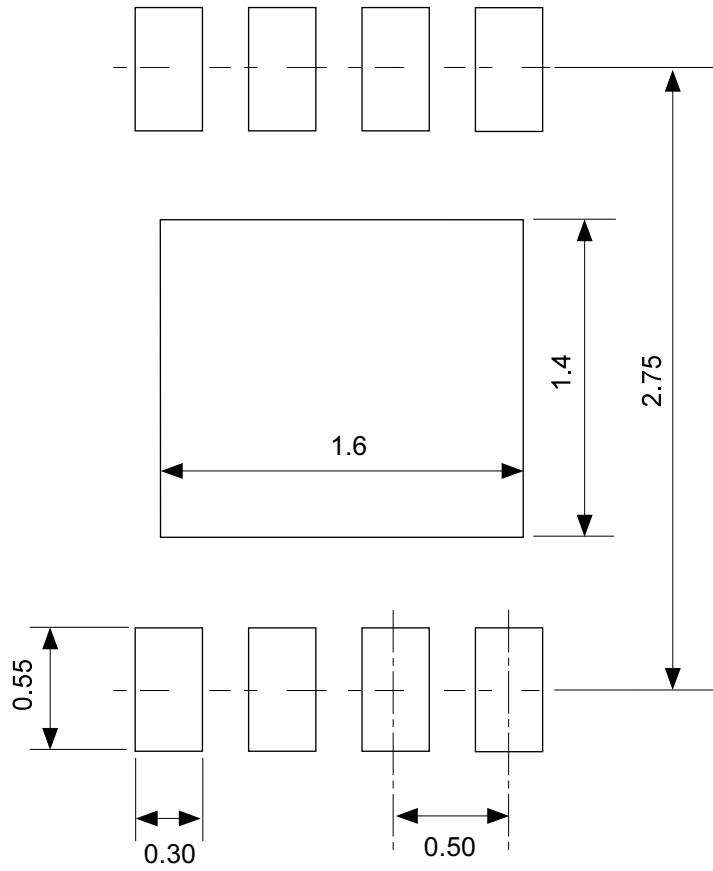


Enlarged drawing in the central part



No. PP008-A-R-SD-2.0

TITLE	HSNT-8-A-Reel		
No.	PP008-A-R-SD-2.0		
ANGLE		QTY.	5,000
UNIT	mm		
<b>ABLIC Inc.</b>			



No. PP008-A-L-SD-1.0

TITLE	HSNT-8-A -Land Recommendation
No.	PP008-A-L-SD-1.0
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	

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2.4-2019.07