

CMOS IC Application Note

S-19113, S-19117/19119, S-191E, S-191L/191N Series **VOLTAGE DETECTOR POWOR ON SEQUENCE**

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This application note is a reference which explains the power on sequence for the below-listed voltage detectors. The waveforms and circuit diagrams in this application note are examples for window voltage detectors. Refer to the datasheets for details and specs of target products.

[Target Products]

- S-19113xxxS Series
- S-19113xxxA Series
- S-19113xxxH Series
- S-19117/19119xxxS Series
- S-19117/19119xxxA Series
- S-19117/19119xxxH Series
- S-191ExxxxS Series*¹
- S-191ExxxxA Series*¹
- S-191ExxxxH Series*¹
- S-191L/191NxxxxS Series*¹
- S-191L/191NxxxxA Series*¹
- S-191L/191NxxxxH Series*¹

*1. Window voltage detector

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1. Startup Operations Resulting from Power on Sequence

1.1 Operations for power on in VDD pin → SENSE pin order or simultaneous VDD pin and SENSE pin power on (under normal conditions)

If power on is carried out in VDD pin → SENSE pin order according to the power on procedures noted in the datasheet, the waveform will be as shown in **Figure 1**, while if power on is carried out simultaneously for the VDD pin and SENSE pin, the waveform will be as shown in **Figure 2**.

If $V_{SENSE} \geq$ release voltage (V_{UVREL}), UV pin output rise after the delay time set in the release delay time adjustment capacitor elapses, and the low voltage detector enter the release status (normal operation).

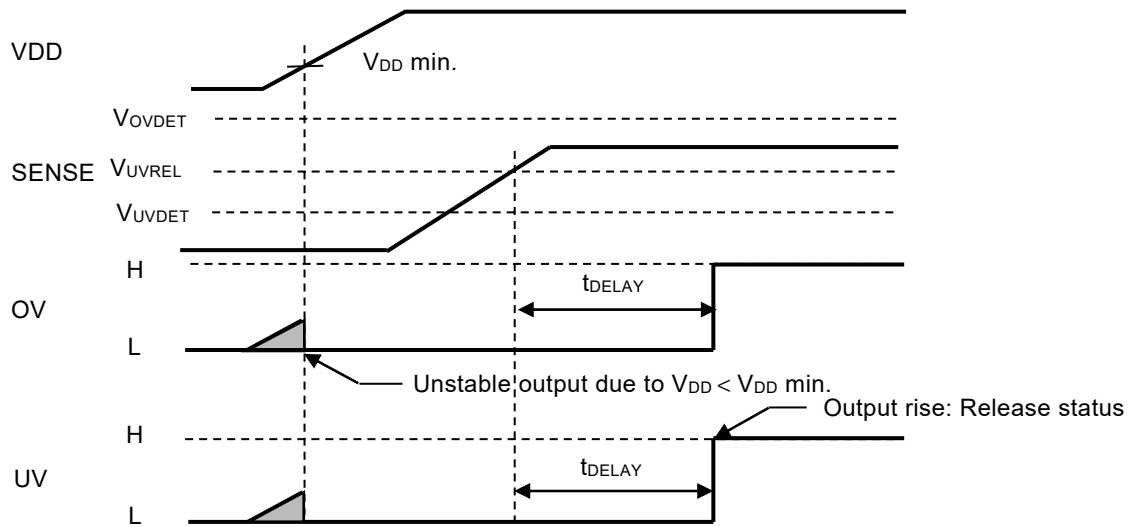


Figure 1

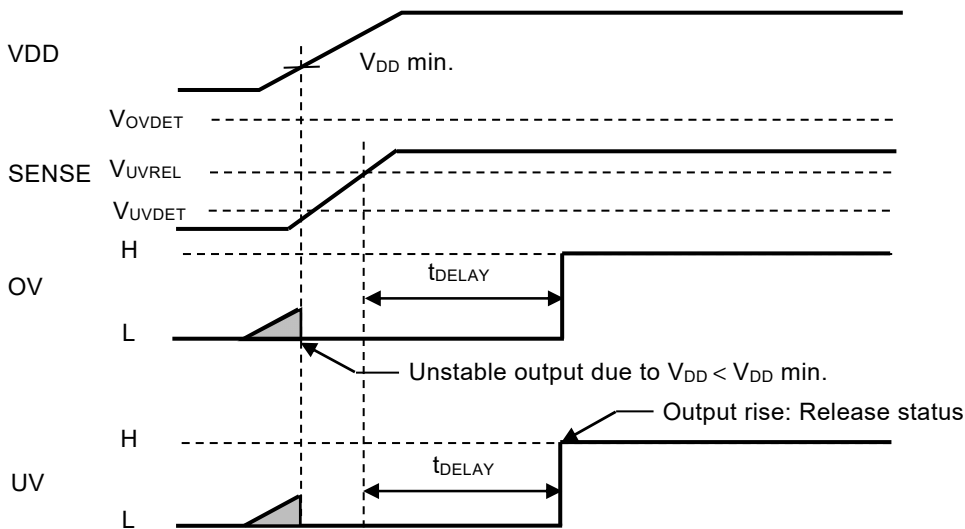


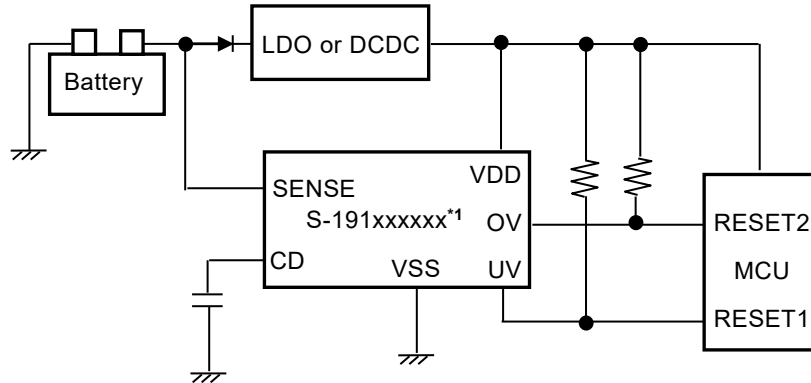
Figure 2

Remark For the S-19113 Series, replace UV pin with OUT pin, and for the S-19117/19119 Series, replace UV pin with RO pin. The S-19113 Series and S-19117/19119 Series have no OV pin.

VOLTAGE DETECTOR POWER ON SEQUENCE

1. 2 Operations for power on in SENSE pin → VDD pin order

In the target products, because the SENSE pin has a reverse connection protection function, it is possible to connect the SENSE pin before the reverse connection protection diode as shown in **Figure 3** to directly monitor the battery. When doing so, if the VDD pin is connected to stepped-down voltage from a separate power supply or the same power supply line, power on will occur in SENSE pin → VDD pin order. SENSE pin applied voltage operation status is explained in 1. 2. 1 to 1. 2. 3.



*1. Refer to [Target products].

Figure 3

1. 2. 1 If $V_{UVREL} \leq V_{SENSE}$ (release status)

If the VDD voltage exceeds the minimum operation voltage ($V_{DD\ min.}$), the internal circuit will operate, and UV pin output rise after the delay time set in the release delay time adjustment capacitor elapses, and the low voltage detector enter the release status (normal operation).

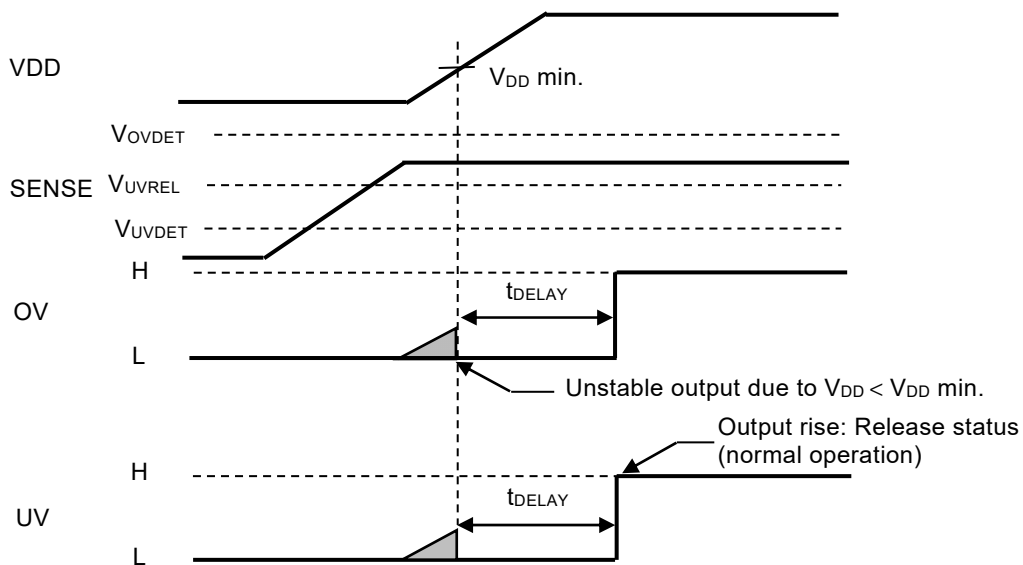


Figure 4

Remark For the S-19113 Series, replace UV pin with OUT pin, and for the S-19117/19119 Series, replace UV pin with RO pin. The S-19113 Series and S-19117/19119 Series have no OV pin.

1. 2. 2 If $V_{UVDET} > V_{SENSE}$ (detection status)

If VDD voltage exceeds the minimum operation voltage ($V_{DD \text{ min.}}$), the internal circuit will operate, and UV pin output will maintain "L", and the low voltage detector enter the detection status (normal operation).

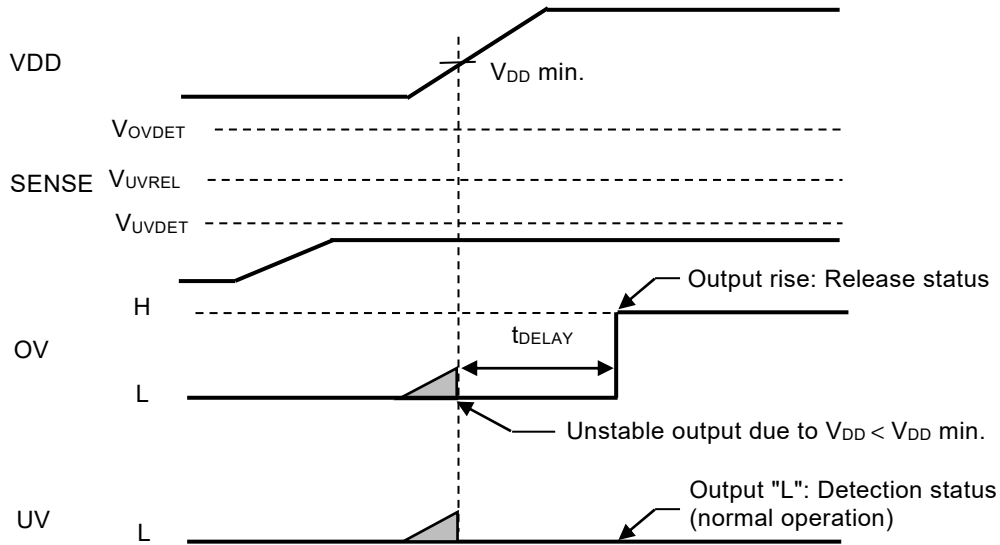


Figure 5

1. 2. 3 If $V_{UVDET} < V_{SENSE} < V_{UVREL}$ (within hysteresis range)

If the following 2 conditions both occur, the switch which configures the hysteresis connected to the SENSE resistance will switch from OFF to ON, causing the UV pin output to switch from "L" (normal expected value) to "H", resulting in the low voltage detector to enter an erroneous release status.

- (1) Steep rise of VDD voltage
- (2) Within hysteresis range

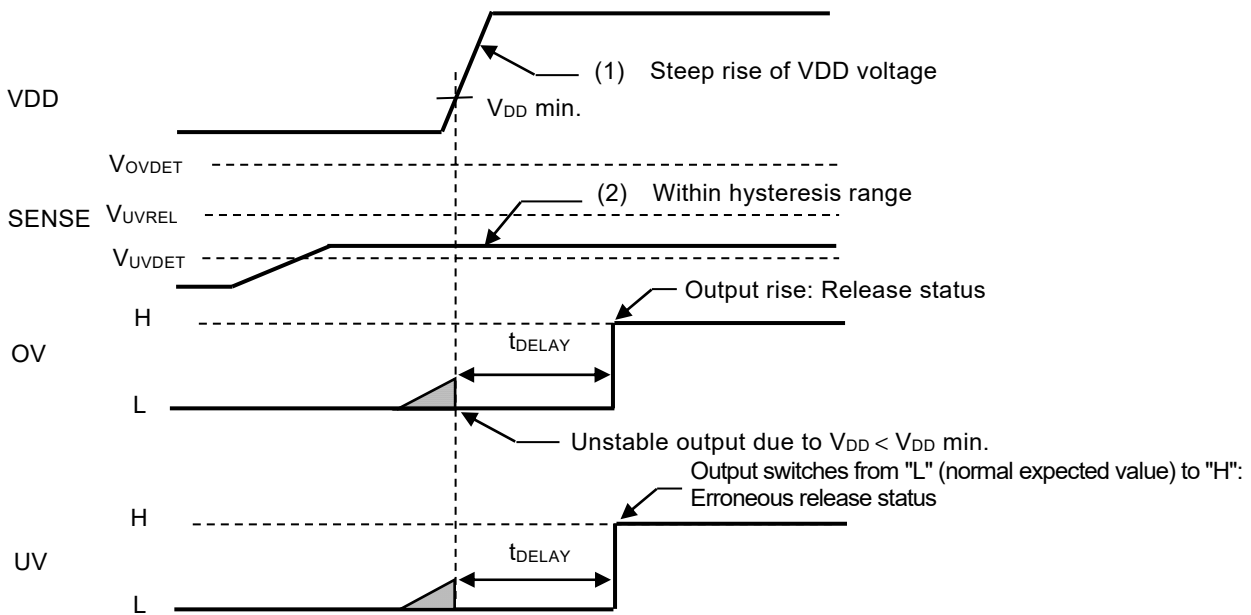


Figure 6

Remark For the S-19113 Series, replace UV pin with OUT pin, and for the S-19117/19119 Series, replace UV pin with RO pin. The S-19113 Series and S-19117/19119 Series have no OV pin.

VOLTAGE DETECTOR POWER ON SEQUENCE

1.3 Countermeasures for erroneous release when power on occurs in SENSE pin → VDD pin order

The following 2 countermeasures are available for the erroneous release status noted in "1.2.3 If $V_{UVDET} < V_{SENSE} < V_{UVREL}$ (within hysteresis range)".

- Use a product with no hysteresis
- Slow the VDD voltage rise speed (refer to Figure 7)

As shown by the dashed line in the Figure 8 as a reference circuit diagram, the VDD voltage rise speed can be slowed by attaching a CR circuit to the VDD pin.

In the target products, feed-through current flows at the time of detection and release. For this reason, if the input impedance is high, oscillation may occur due to voltage drop caused by the feed-through current. It is recommended to decrease R_{IN} . Perform thorough evaluation including the temperature characteristics with an actual application to select C_{IN} and R_{IN} .

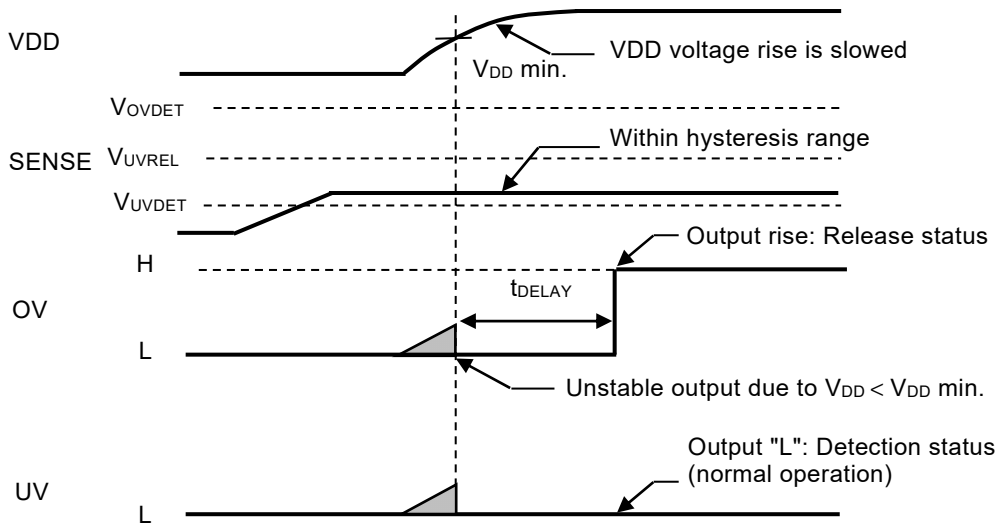
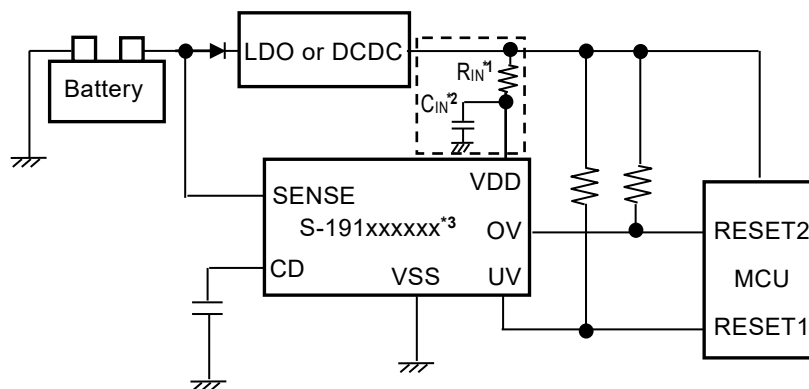


Figure 7



- *1. $R_{IN} = 200 \Omega$ (Reference value)
- *2. $C_{IN} = 0.47 \mu F$ (Reference value)
- *3. Refer to [Target products].

Figure 8

Remark For the S-19113 Series, replace UV pin with OUT pin, and for the S-19117/19119 Series, replace UV pin with RO pin. The S-19113 Series and S-19117/19119 Series have no OV pin.

2. Precautions

- The usages described in this application note are typical examples using ICs of ABLIC Inc. Perform thorough evaluation before use.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
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3. Related Sources

Refer to the following datasheets for details of target products.

S-19113xxxS Series Datasheet
S-19113xxxA Series Datasheet
S-19113xxxH Series Datasheet
S-19117/19119xxxS Series Datasheet
S-19117/19119xxxA Series Datasheet
S-19117/19119xxxH Series Datasheet
S-191ExxxxS Series Datasheet
S-191ExxxxA Series Datasheet
S-191ExxxxH Series Datasheet
S-191L/191NxxxS Series Datasheet
S-191L/191NxxxA Series Datasheet
S-191L/191NxxxH Series Datasheet

The information described in this application note and the datasheet is subject to change without notice.

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