CMOS IC Application Note

Parallel Operation of S-19682B/19683B Series

Rev.1.0_00

This application note is a reference describing applications of parallel operation of the S-19682B/19683B Series (high side switch).
Refer to the datasheets for details and specs of these ICs.

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1. The Purpose of Parallel Operation

1. 1 Increasing output current

When a high side switch is operated singly, the limit current (I_{LIM}) determines output load drive capability.
For example, single operation of the S-19683B Series with a set limit current ($I_{LIM(S)}$) of 600 mA provides an output current of 600 mA typ. When two or more high-side switches are operated in parallel, the overall output load drive capability can be greater than in single operation. For example, parallel operation of two S-19683B Series devices with a set limit ($I_{LIM(S)}$) of 600 mA provides an output current of 1200 mA typ.
When single operation of a high side switch does not provide enough output current, parallel operation of two switches can be used to compensate. For this reason, parallel operation should be used for high load current applications.

1. 2 Controlling heat build-up

When multiple high side switches are used in parallel operation to distribute current flowing to the load, the on-resistance of the internal switches reduces voltage drops.
The reduction of voltage drops lowers both the power and the resulting heat generated in the IC. This reduces increases in temperature caused by heat in the IC and the board. In applications with a high ambient temperature, adequate heat dissipation may not be obtained in some mounting conditions. Parallel operation is effective as a means to ensure that the maximum temperature of the IC junction is not exceeded.
Figure 1 shows a simplified equivalent circuit of a high side switch in single operation and **Figure 2** shows a similar equivalent circuit of two high side switches in parallel operation. The simplification ignores the wiring resistance of the mounted boards and the on-resistance of the two high side switches is assumed to be identical (both R_{ON}).
The overall on-resistance during parallel operation is $\frac{R_{ON}}{2}$. In parallel operation, half the load current of that in single operation $\left(\frac{I_{LOAD}}{2}\right)$ flows to each IC, and as power is $\left(\frac{I_{LOAD}}{2}\right)^2 \times R_{ON}$, the power generated in each IC is 1/4 of that in single operation. Since the power used in parallel operation is half that of single operation, heat generation is also about half.

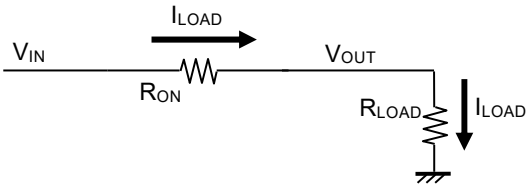


Figure 1

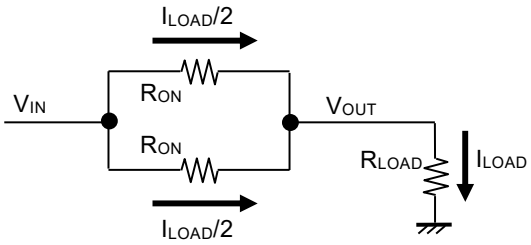


Figure 2

2. Making Parallel Connections

This section describes how to appropriately connect high side switches to operate them in parallel.
Make a parallel connection to two high side switches as shown in **Figure 3** to operate them in parallel. To operate three or more high side switches in parallel, interconnect the IC pins of the third and subsequent ICs as shown in **Figure 3**.

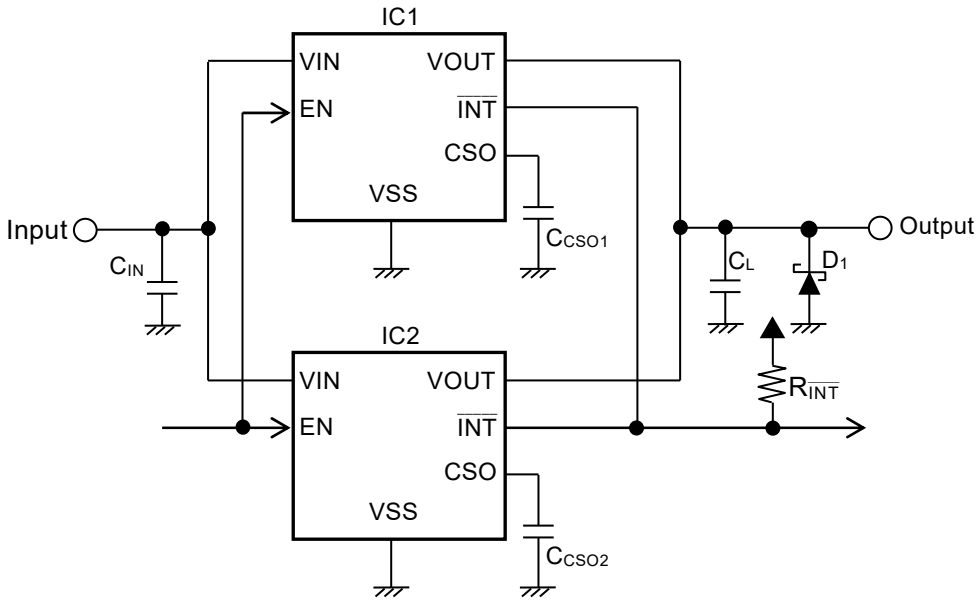


Figure 3 Example Showing Parallel Connection of Two ICs

Caution 1. To stabilize the current balance between the ICs, the CSO pin of each IC must not be interconnected. Also, connect a capacitor to the CSO pin of each IC to stabilize CSO pin output.
2. As shown in Figure 3, the capacitor for stabilizing the input (C_{IN}), the capacitor for stabilizing the output (C_L) and the protection Schottky-barrier diode (D_1) can be shared, but the ICs should be placed close together and C_{IN}, C_L and D_1 should be located as close to the IC connection pins as possible.
3. The above connection diagram will not guarantee successful operation.
Perform thorough evaluation using the actual application to set the constants.

3. Description of Parallel Operation

3. 1 Balancing current (during switch operation)

This section describes how the current in parallel operation is balanced during the switch operation of each IC.
In **Figure 2** in "**1. Purpose of Parallel Operation**", wiring resistance of the mounted board is ignored, and the on-resistance of the two high-side switches is assumed to be identical. However, in reality, wiring resistance of the mounted board exists, and on-resistance varies depending on the individual differences. **Figure 4** shows an equivalent circuit of parallel operation of high side switch IC1 and IC2 that takes these factors into account.

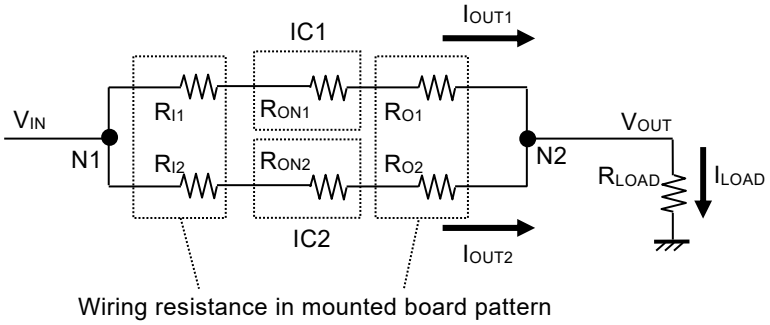


Figure 4

The wiring on the VIN pin side comes together at contact point N1 and the wiring on the VOUT pin side comes together at contact point N2. Thus, the combined resistance on the IC1 side (R_1) and the combined resistance on the IC2 side (R_2) of the path between N1 and N2 are as shown in equations (1) and (2), respectively.

$$R_1 = R_{I1} + R_{ON1} + R_{O1} \quad \text{.....(1)}$$
$$R_2 = R_{I2} + R_{ON2} + R_{O2} \quad \text{.....(2)}$$

Remark R_{ON1}: On-resistance for IC1
R_{ON2}: On-resistance for IC2
R_{I1}: Wiring resistance on the VIN pin side of IC1
R_{I2}: Wiring resistance on the VIN pin side of IC2
R_{O1}: Wiring resistance on the VOUT pin side of IC1
R_{O2}: Wiring resistance on the VOUT pin side of IC2

At this time, the ratio of output current (I_{OUT1}) at the IC1 side and output current (I_{OUT2}) at the IC2 side is expressed by equation (3).

$$\frac{I_{OUT1}}{I_{OUT2}} = \frac{1 + \frac{R_2}{R_1}}{1 + \frac{R_1}{R_2}} \quad \text{.....(3)}$$

When $\frac{I_{OUT1}}{I_{OUT2}} = 1$, the output current of each IC is matched. Equation (3) indicates that the smaller the difference between R_1 and R_2, the closer $\frac{I_{OUT1}}{I_{OUT2}}$ is to 1, and the better the current balance becomes.
An example of a current balance calculation is shown below.

If R_{ON1} is 610 mΩ, R_{ON2} is 620 mΩ and R_{I1}, R_{I2}, R_{O1}, R_{O2} are 2 mΩ,
R_1 = 614 mΩ, R_2 = 624 mΩ
$\frac{I_{OUT1}}{I_{OUT2}}$ = 1.0163

Then the percentage difference in current between the IC1 and IC2 paths is +1.63%.

To calculate the current balance in an actual application, calculate the wiring resistance of the mounting board from the board pattern. Refer to **Figure 5** for information on variations in on-resistance of the S-19682B/19683B Series.

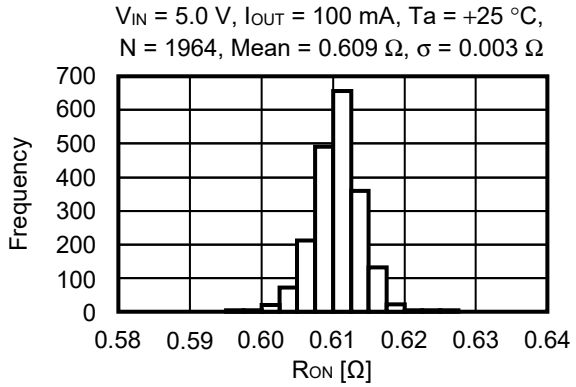


Figure 5

Remark N: Number of samples

3. 2 Balancing current (when limiting overcurrent)

This section describes the current balance when each IC in parallel is operating at the overcurrent limit.
Figure 6 shows an equivalent circuit of overcurrent limiting during parallel operation of the two high side switches IC1 and IC2.

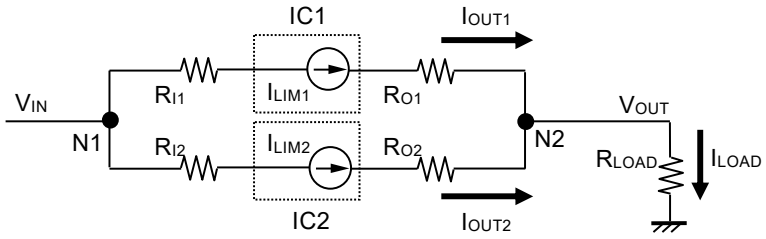


Figure 6

When each IC is limiting overcurrent, the output current of IC1 (I_{OUT1}) becomes the limit current (I_{LIM1}) determined internally by IC1, and the output current of IC2 (I_{OUT2}) becomes the limit current (I_{LIM2}) determined internally by IC2. Therefore, the current balance during overcurrent limiting can be expressed by equation (4).

$$\frac{I_{OUT1}}{I_{OUT2}} = \frac{I_{LIM1}}{I_{LIM2}} \quad \text{.....(4)}$$

Regardless of whether the ICs operate singly or in parallel, the limit current of each IC is the value given in the "■ **Electrical Characteristics**" section of the datasheet. Refer to **Figure 7** and **Figure 8** for information on variations in the limit current of the S-19682B/19683B Series.
The overall limit current in parallel operation is determined by the sum of the limit currents of each IC connected in parallel. In **Figure 6**, it is $I_{LIM1} + I_{LIM2}$.

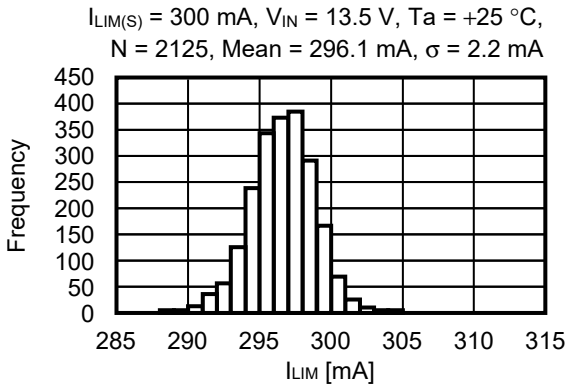


Figure 7 S-19682B Series

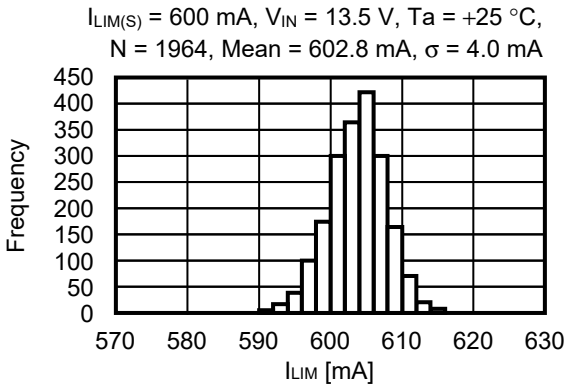


Figure 8 S-19683B Series

Remark N: Number of samples

The following explains the change from switch operation to limiting overcurrent while taking into account the variations in limit current shown in **Figure 7** and **Figure 8**. The example below assumes that $I_{LIM1} > I_{LIM2}$.
When the load current (I_{LOAD}) increases and I_{OUT2} reaches I_{LIM2}, IC2 first starts to limit overcurrent, while IC1 remains in switch operation. At this time, the output voltage (V_{OUT}) = $V_{IN} - R_1 \times I_{OUT1}$. When the load current increases further and I_{OUT1} reaches I_{LIM1}, IC1 also starts to limit overcurrent. When both IC1 and IC2 are limiting overcurrent, $V_{OUT} = R_{LOAD} \times (I_{LIM1} + I_{LIM2})$.

3. 3 Thermal shutdown circuit

This section describes the operation of the thermal shutdown circuit during parallel operation.
When the IC1 and IC2 high side switches are operating in parallel, the thermal shutdown circuit of each IC operates independently. For example, if IC1 heats up first and causes the thermal shutdown circuit to enter detection status, the output of IC1 is turned off and the load current flows only to IC2 whose output stays on. Therefore, the overall output load drive capability depends on IC2, the remaining IC. When the load current exceeds the IC2 limit current, overcurrent limiting starts. As V_{OUT} drops and heat generation increases during overcurrent limiting, there is a possibility that also the IC2 thermal shutdown circuit may enter detection status. When the thermal shutdown circuits of both IC1 and IC2 enter detection status, the outputs of IC1 and IC2 are turned off to limit heat generation.

3. 4 Electrical characteristics

When the S-19682B/19683B Series is operated in parallel, the electrical characteristics of each IC are as stated in the datasheet. **Table 1** shows the electrical characteristics when the S-19683B Series is operated singly and the overall electrical characteristics when n*1 number of S-19683B Series ICs with the same set limit current ($I_{LIM(S)}$) is operated in parallel.
When considering parallel operation, make sure to confirm that the application can handle the overall electrical characteristics of parallel operation.

Table 1

Item*2	Symbol	Single Operation		Parallel Operation (n)		Unit
		Min.	Max.	Min.	Max.	
Current consumption during operation	I_{SS1}	–	95	–	$95 \times n$	μA
Current consumption during power-off	I_{SS2}	–	2.0	–	$2.0 \times n$	μA
ON resistance	R_{ON}	–	1.0	–	$\frac{1.0}{n}$	Ω
Output OFF leakage current	$I_{LEAK,VOUT}$	–	2.0	–	$2.0 \times n$	μA
Limit current	I_{LIM}	$I_{LIM(S)} \times 0.9$	$I_{LIM(S)} \times 1.1$	$I_{LIM(S)} \times 0.9 \times n$	$I_{LIM(S)} \times 1.1 \times n$	mA
Interrupt output leakage current	$I_{LEAK,\overline{INT}}$	–	1.0	–	$1.0 \times n$	μA
EN pin input current "H"	I_{SH}	–	1.0	–	$1.0 \times n$	μA
EN pin input current "L"	I_{SL}	–0.2	0.2	$-0.2 \times n$	$0.2 \times n$	μA

***1.** n: An integer greater than or equal to 2
***2.** Refer to the datasheet for information on the measurement conditions of each item.

3. 5 Connection diagnosis function

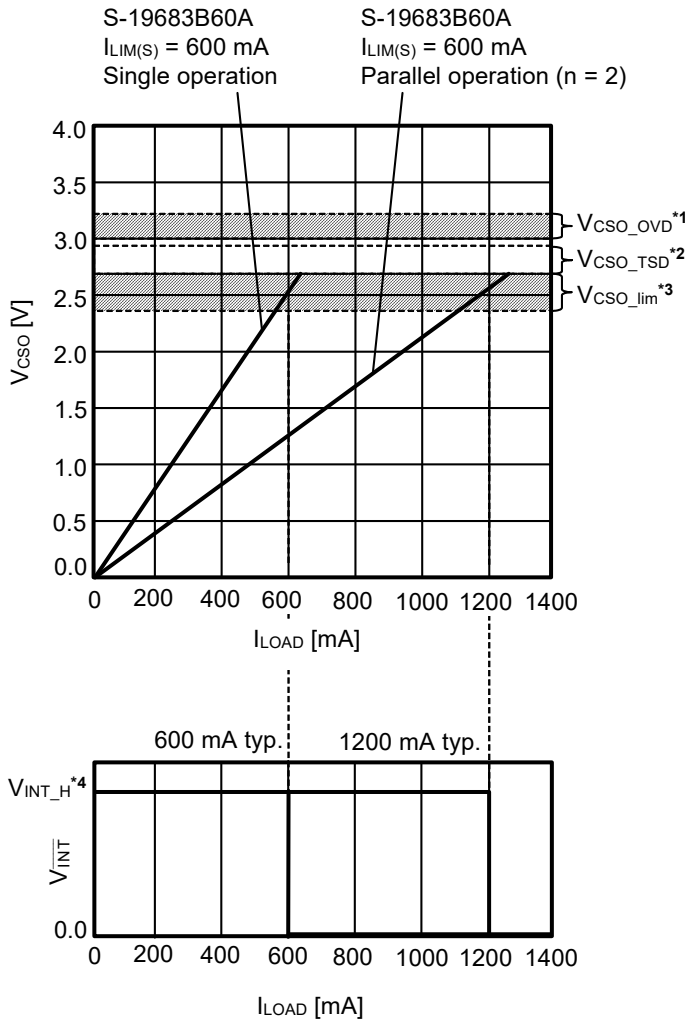
The S-19682B/19683B Series can use the CSO pin and the $\overline{INT}$ pin to monitor current and detect operating status. This section describes each function of parallel operation.

Figure 9 shows an example of the output of the CSO pin and the $\overline{INT}$ pin when the S-19683B Series with the set limit current ($I_{LIM(S)}$) of 600 mA is operated singly and when two S-19683B Series are operated in parallel.

Since the CSO pin voltage (V_{CSO}) is proportional to the load current (I_{LOAD}), V_{CSO} for parallel operation is 1/2 as large as V_{CSO} for single operation. At this time, the current differences between each IC are included in V_{CSO} as described in "**3. 1 Balancing current (during switch operation)**". When V_{CSO} reaches the CSO pin current limit voltage (V_{CSO_lim}), the IC enters current limiting status.

When a parallel connection is performed as shown in **Figure 3** in "**2. Making Parallel Connections**", V_{CSO} on either IC1 or IC2 can be monitored. Monitoring the V_{CSO} of both ICs makes it possible to monitor the current of each IC during parallel operation.

The $\overline{INT}$ pin of the S-19682B/19683B Series is an Nch open-drain output and can therefore be wired-OR connected as shown in **Figure 3**. The $\overline{INT}$ pin goes to "L" when a parallel-connected IC enters overcurrent, overheat, or overvoltage status.



***1.** Output voltage during overvoltage detection of CSO pin
***2.** Output voltage during thermal shutdown detection of CSO pin
***3.** Current limit voltage for CSO pin
***4.** Pull-up voltage

Figure 9

Caution Do not interconnect CSO pins on ICs connected in parallel when using the CSO pin for current monitoring.

4. Board Layout for Parallel Connections

When connecting the S-19682B/19683B Series in parallel, current must be properly balanced between each IC to prevent concentration of current in the path of a specific IC (refer to the "**3. 1 Balancing current (during switch operation)**").
For this reason, design the board pattern so that the resistance values in the wiring connecting the VIN pin and VOUT pin of each IC are the same.
Specifically, connect the VIN pin and VOUT pin of each IC as close to each other as possible. Also, in order to reduce the impact of wiring resistance differences on current balance, increase the width of the wiring connecting the VIN pin and VOUT pin to lower the wiring resistance value.
Figure 10 shows a good example of how the VIN pin and VOUT pin should be wired in the layout of a board in a parallel connection. The good example takes current balance into account in the wiring of IC1 and IC2 so that wiring resistance on the IC1 and IC2 sides is the same. **Figure 11** shows a bad example. In the bad example, wiring resistance on the IC1 side is too low, while it is too large on the IC2 side resulting in poorer current balance than the example in **Figure 10**.

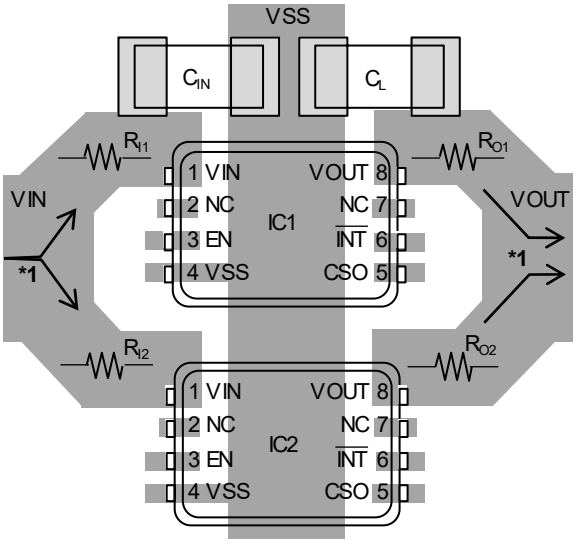


Figure 10 Good Example

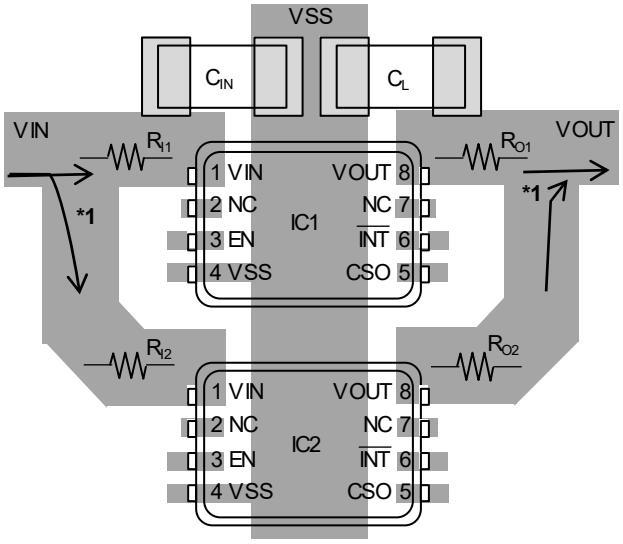


Figure 11 Bad Example

***1.** The arrows indicate the direction of current flow.

5. Precautions

- The usages described in this application note are typical examples using ICs of ABLIC Inc.
  Perform thorough evaluation before use.

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

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6. Related Sources

Refer to the following datasheets for details of the S-19682B/19683B Series.

S-19682B Series Datasheet
S-19683B Series Datasheet

The information described in this application note and the datasheet is subject to change without notice.
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