

# Operation

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The S-8471 Series and the S-8474 Series are wireless power ICs.

The S-8471 Series is a receiver control IC (Receiver), and the S-8474 Series is a transmitter control IC (Transmitter). This application note serves as technical documentation that describes the combined operation and characteristics of the S-8471 Series and S-8474 Series.

Refer to the S-8471 Series and S-8474 Series datasheets for additional details.

- Caution 1. Wireless power transfer devices which use the S-8471 Series and S-8474 Series are optimized to operate at LC resonant frequencies of approximately 88kHz to 106kHz. Within the 88kHz to 106kHz LC resonant frequency range, the circuit for detecting the receiver control IC operates, and the transmitter control IC also operates correctly. If the constants of the used coil (L) and capacitor (C) are changed, the LC resonant frequency also will change, so make sure to maintain the LC resonant frequency within the 88kHz to 106kHz range.
  - 2. There is polarity to the receiver coil and transmitter coil in wireless power transfer devices which use the S-8471 Series and S-8474 Series. Combine receiver coils and transmitter coils according to the details in this application note.

## 2. Operation

This application note describes the combined circuit operation of the S-8471 Series and S-8474 Series, as shown in **Figure 8.** 

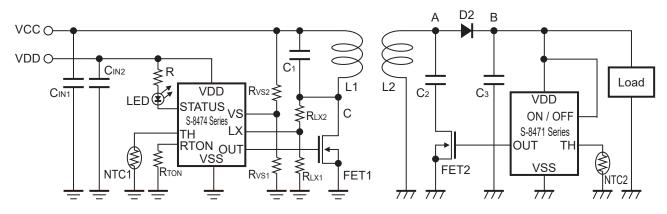
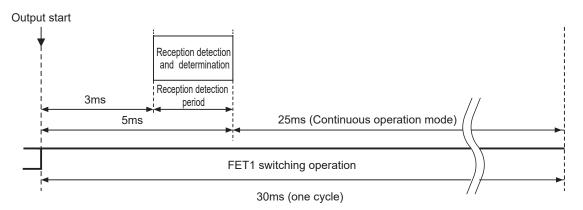


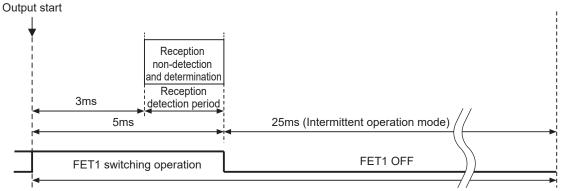
Figure 8 Recommended Circuit

#### 2.1 Reception detection and operation mode of transmitter

The transmitter has two operation modes: continuous operation mode and intermittent operation mode. Switching between the continuous operation mode and the intermittent operation mode is determined by the reception detection (within 3ms typ. to 5ms typ.) after output start. This result determines the mode within the remaining 25ms typ. The determination of switching between the continuous operation and intermittent operation modes is made repeatedly every 30ms typ. (one cycle). The LED connected to STATUS pin lights up when power reception is detected continuously for 16 cycles. In the same manner, the LED turns off when power reception is not detected continuously for 16 cycles.







30ms (one cycle)

Figure 10 Intermittent Operation Mode (typ.)
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#### 2.2 Reception detection mechanism of transmitter

Reception is detected by comparing the peak values of the transmitter LX pin voltage waveform.

When mutual induction occurs between the transmitter and the receiver, the receiver performs constant voltage control. Thus FET2 turns ON and OFF repeatedly due to switching operation. The switching of FET2 between ON and OFF changes the peak values of the transmitter LX pin voltage.

As shown in **Figure 11**, when the difference between these waveform peak values reaches approximately 0.1V<sup>\*1</sup> or higher, the transmitter acknowledges that reception has been detected and transitions to continuous operation mode.

Note that in the following cases, the difference between waveform peak values decreases and the transmitter will not transition to continuous operation mode.

- Load is too light
- Load is too heavy
- Presence of the receiver cannot be confirmed
- Distance between coils is too close

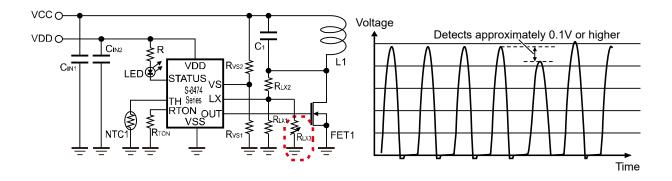


Figure 11 LX Pin Voltage Waveform

\*1. Because the difference between waveform peak values cannot be directly measured, use the following method to find the difference.

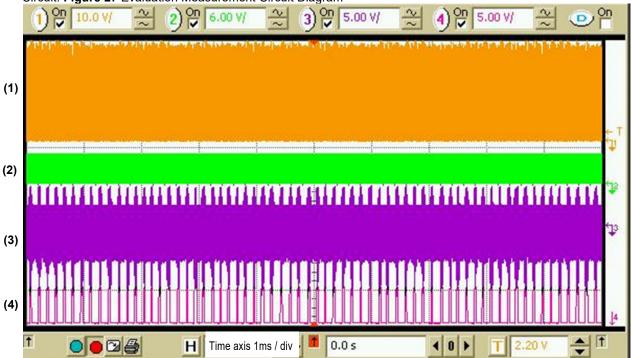
Change R<sub>LX3</sub> from **Figure 11** while synchronizing it to the OUT output and detect the point at which it switches to continuous operation mode.

The peak value difference varies depending on coil wire length and other variables, so use 0.1V as a reference value.

## 2. 3 Transmitter coil, transmitter FET control, receiver coil, receiver FET control waveforms (Continuous operation mode)

**Figure 12** and **Figure 13** show each waveform during continuous operation. The receiver VDD voltage (not shown in the figure) transitions between  $V_{OVP}$  and  $(V_{OVP} - V_{HYS})$ , and receiver FET2 gate waveform changes to "H" and "L" repeatedly, while the transmitter performs continuous operation.

Conditions: Perpendicular distance between coils (d) = 4mm,  $V_{DD}$  = 5V,  $V_{CC}$  = 9V,  $I_{OUT}$  = 30mA, Circuit: **Figure 27** Evaluation Measurement Circuit Diagram

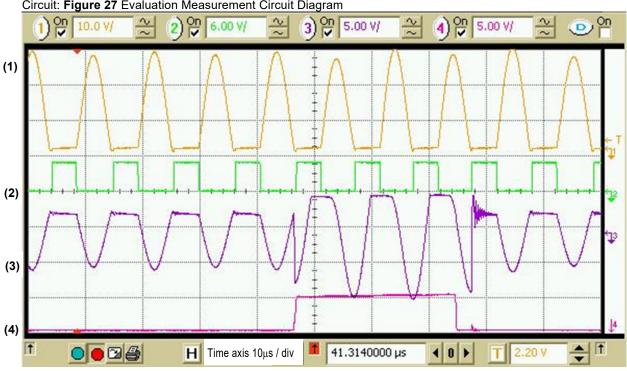


(1) Transmitter coil waveform at point C (10V / div)

(2) Transmitter FET1 gate waveform (6V / div)

(3) Receiver coil waveform at point A (5V / div)





Conditions: Perpendicular distance between coils (d) = 4mm,  $V_{DD}$  = 5V,  $V_{CC}$  = 9V,  $I_{OUT}$  = 30mA, Circuit: **Figure 27** Evaluation Measurement Circuit Diagram

(1) Transmitter coil waveform at point C (10V / div)

(2) Transmitter FET1 gate waveform (6V / div)

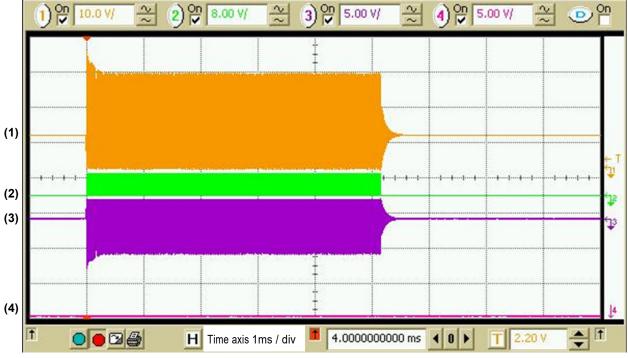
(3) Receiver coil waveform at point A (5V / div)

Figure 13 Waveforms during Continuous Operation Mode (Enlarged Figure)

## 2. 4 Transmitter coil, transmitter FET control, receiver coil, receiver FET control waveforms (Intermittent operation mode)

**Figure 14** and **Figure 15** show each waveform during intermittent operation. The transmitter performs intermittent operation when the receiver VDD voltage (not shown in the figure) is over V<sub>OVP</sub> due to a light load and receiver FET2 gate waveform maintains "L".

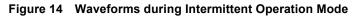
Conditions: Perpendicular distance between coils (d) = 4mm, V<sub>DD1</sub> = 5V, V<sub>CC</sub> = 9V, I<sub>OUT</sub> = 0mA (Without load), Circuit: **Figure 27** Evaluation Measurement Circuit Diagram

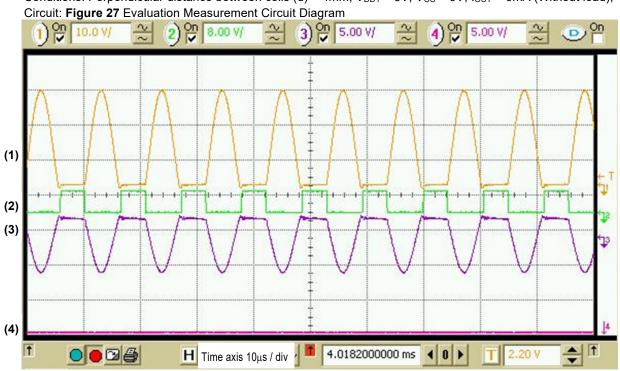


(1) Transmitter coil waveform at point C (10V / div)

(2) Transmitter FET1 gate waveform (8V / div)

(3) Receiver coil waveform at point A (5V / div)





Conditions: Perpendicular distance between coils (d) = 4mm, V<sub>DD1</sub> = 5V, V<sub>CC</sub> = 9V, I<sub>OUT</sub> = 0mA (Without load),

(1) Transmitter coil waveform at point C (10V / div)

(2) Transmitter FET1 gate waveform (8V / div)

(3) Receiver coil waveform at point A (5V / div)

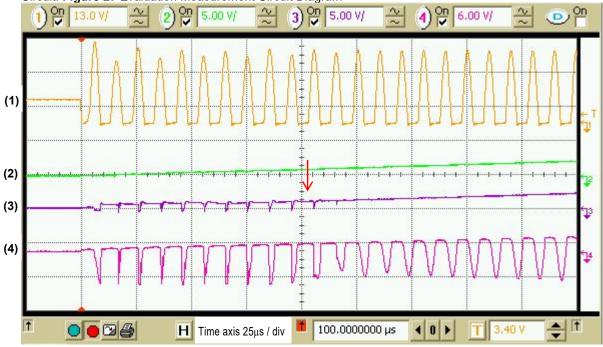


#### 2.10 Operation of receiver

#### 2. 10. 1 Initial status of reception

**Figure 19** shows the LC waveform at point C of the transmitter and each waveform of the receiver in the initial status of reception. The receiver VDD voltage rises due to mutual induction, and the receiver FET2 gate voltage exceeds the FET2 threshold voltage while FET2 is turned ON from the timing illustrated by the arrow in **Figure 19**. As a result,  $C_2$  becomes connection status and the receiver starts LC resonance.

Conditions: Perpendicular distance between coils (d) = 4mm,  $V_{DD1}$  = 5V,  $V_{CC}$  = 9V,  $I_{OUT}$  = 30mA, Circuit: **Figure 27** Evaluation Measurement Circuit Diagram



(1) Transmitter LC waveform at point C (13V / div)

(2) Receiver VDD waveform at point B (5V / div)

(3) Receiver FET2 gate waveform (5V / div)

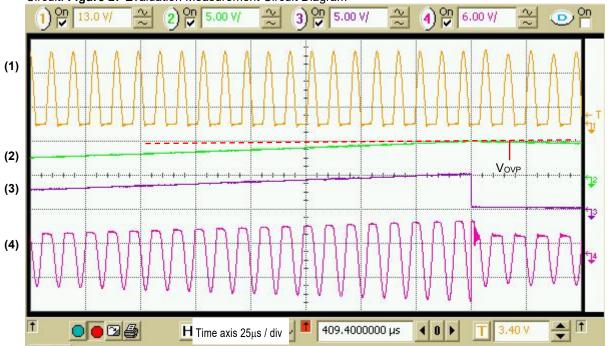
(4) Receiver LC waveform at point A (6V / div)



#### 2. 10. 2 Status when overvoltage detection voltage (VovP) is reached

**Figure 20** shows each waveform in the status when receiver VDD voltage reaches  $V_{OVP}$ . The receiver VDD voltage rises due to the receiver LC resonance which continues from the initial status of reception. When it reaches  $V_{OVP}$ , "L" is output from the receiver OUT pin, and receiver FET2 is turned OFF. As a result, C<sub>2</sub> becomes open and the receiver stops LC resonance.

Conditions: Perpendicular distance between coils (d) = 4mm,  $V_{DD1}$  = 5V,  $V_{CC}$  = 9V,  $I_{OUT}$  = 30mA, Circuit: **Figure 27** Evaluation Measurement Circuit Diagram



(1) Transmitter LC waveform at point C (13V / div)

(2) Receiver VDD waveform at point B (5V/ div)

(3) Receiver FET2 gate waveform (5V / div)

(4) Receiver LC waveform at point A (6V / div)

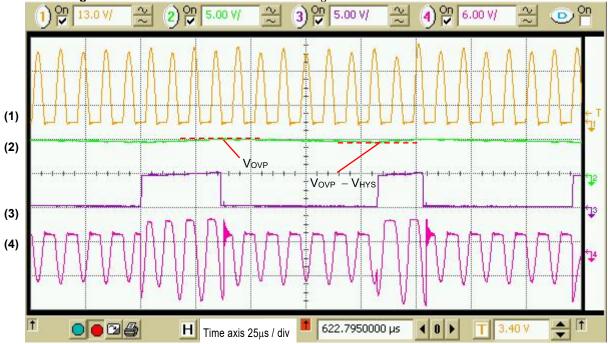


#### 2. 10. 3 Stable status

As shown in "Figure 6 Relation between Receiver FET2 Control and Receiver VDD Voltage (Conceptual Diagram)", after receiver VDD voltage (point B) reaches V<sub>OVP</sub>, it transitions between V<sub>OVP</sub> and V<sub>OVP</sub> – V<sub>HYS</sub> since receiver FET2 is repeatedly turned ON and OFF.

As shown in **Figure 21**, repeatedly turning receiver FET2 ON and OFF also causes the peak values of the transmitter LC waveform to change and the transmitter to enter the continuous operation mode.

Conditions: Perpendicular distance between coils (d) = 4mm,  $V_{DD1}$  = 5V,  $V_{CC}$  = 9V,  $I_{OUT}$  = 30mA, Circuit: **Figure 27** Evaluation Measurement Circuit Diagram



(1) Transmitter LC waveform at point C (13V / div)

(2) Receiver VDD waveform at point B (5V / div)

(3) Receiver FET2 gate waveform (5V / div)

(4) Receiver LC waveform at point A (6V / div)

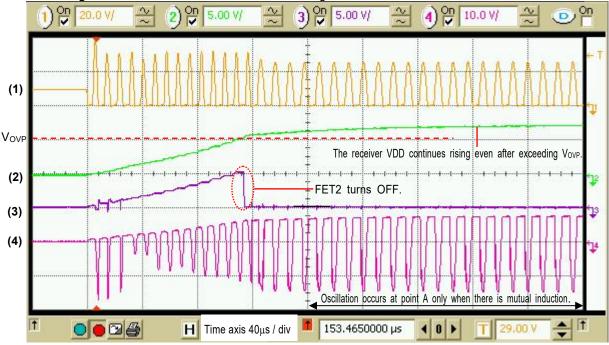
Figure 21 Waveforms in Stable Status

#### 2. 11 Distance between transmitter coil and receiver coil

The coil coupling coefficient changes depending on the distance between the transmitter coil and receiver coil. The coupling coefficient increases if the transmitter coil and the receiver coil are too close together, and even if receiver FET2 is turned OFF, the power is transferred due to mutual induction only. **Figure 22** and **Figure 24** show this phenomenon.

Note as shown in **Figure 22** the receiver VDD voltage may exceed the IC rating if it continues to rise even after exceeding  $V_{OVP}$ .

Conditions: Perpendicular distance between coils (d) = 0mm,  $V_{DD1}$  = 5V,  $V_{CC}$  = 9V,  $I_{OUT}$  = 30mA, Circuit: **Figure 27** Evaluation Measurement Circuit Diagram



(1) Transmitter LC waveform at point C (20V / div)

(2) Receiver VDD waveform at point B (5V / div)

(3) Receiver FET2 gate waveform (5V / div)

(4) Receiver LC waveform at point A (10V / div)

#### Figure 22 Voltage Rising due to Mutual Induction Only

When the receiver VDD voltage is at risk of exceeding the IC rating, connect a Zener diode as shown in **Figure 23**. In that case, the following condition needs to be satisfied.

V<sub>OVP</sub> < Breakdown voltage < IC rated voltage</li>

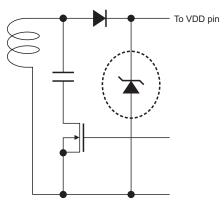
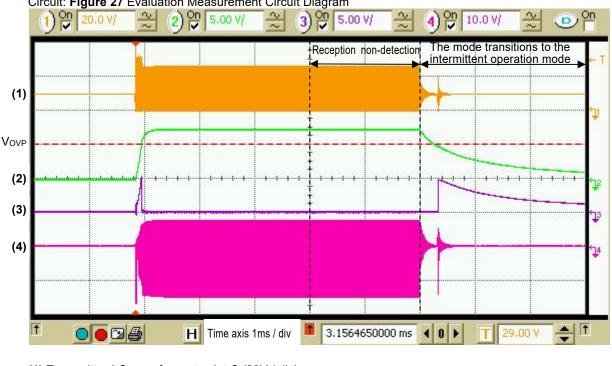


Figure 23 ABLIC Inc. As shown in **Figure 24**, when the receiver VDD voltage reaches  $V_{OVP}$  or higher, "L" is output from the receiver OUT pin, and receiver FET2 remains OFF. Note that at this time, since the waveform of the transmitter LC resonance peak values do not change, the transmitter cannot detect the reception and transitions to intermittent operation mode.



Conditions: Perpendicular distance between coils (d) = 0mm,  $V_{DD1}$  = 5V,  $V_{CC}$  = 9V,  $I_{OUT}$  = 30mA, Circuit: **Figure 27** Evaluation Measurement Circuit Diagram

(1) Transmitter LC waveform at point C (20V / div)

(2) Receiver VDD waveform at point B (5V / div)

(3) Receiver FET2 gate waveform (5V / div)

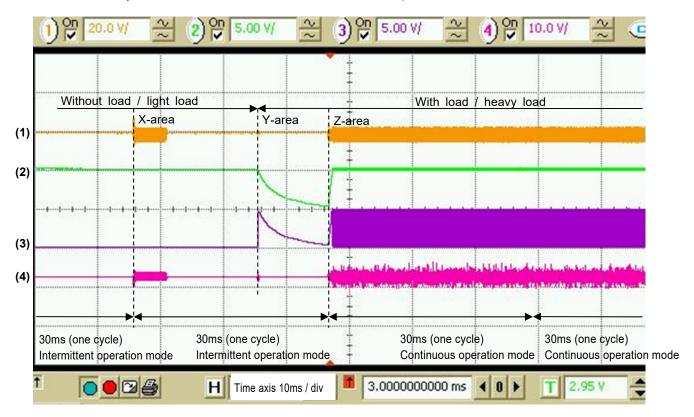
(4) Receiver LC waveform at point A (10V / div)

Figure 24 Receiver VDD Voltage Rising due to Mutual Induction and FET2 Gate Waveform

#### 2.12 Waveforms during transmitter mode switching due to load fluctuation

Figure 25 shows an example of a transition from intermittent operation mode due to light load to continuous operation mode due to load fluctuations.

After operation for the first 5ms typ. in X area, intermittent operation mode is maintained. When load fluctuation occurs in the Y area during the intermittent operation mode period, load is detected during the first 5ms typ. in Z area of the next cycle, and the transmitter transitions to continuous operation mode.



(1) Transmitter LC waveform at point C (20V / div)

(2) Receiver VDD waveform at point B (5V / div)

(3) Receiver FET2 gate waveform (5V / div)

(4) Receiver LC waveform at point A (10V / div)

#### Figure 25 Waveforms during Transmitter Mode Switching due to Load Fluctuation

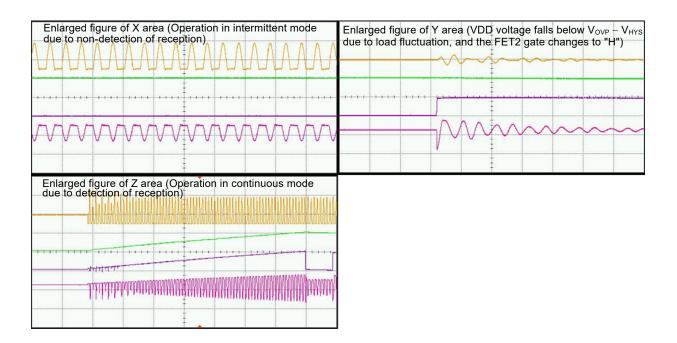


Figure 26 Enlarged Figure of X, Y and Z Areas

### 6. Board Design Considerations

- When wiring a board, make a single GND as described in the S-8471 Series and the S-8474 Series datasheets.
- To protect from overheat, be sure to connect an NTC thermistor to the TH pin for its use.
- For VCC in **Figure 49**, do not use a power supply which might cause frequency component amplitude of 1kHz to 110kHz (LC resonant frequency). It may result in a malfunction.
- For VDD in **Figure 49**, do not use a power supply which might cause frequency component amplitude to prevent from malfunction.
- When designing the board in **Figure 49**, for the following reasons, do not place a wiring near the RTON pin, the VS pin, and the TH pin. Layout so that resistor R<sub>TON</sub> is as close to the RTON pin as possible.
  - (1) Due to coil L1 and resonant capacitor (C1), large voltage fluctuation is generated at point C.

(2) Since impedance in the RTON pin, the VS pin, and the TH pin is high, they are easily affected by an extraneous signal.

By connecting  $C_{RTON}$  (approximately 100pF to 1000pF) between the RTON pin and GND,  $C_{VS}$  (approximately 100pF to 1000pF) between the VS pin and GND and  $C_{NTC}$  (approximately 100pF to 1000pF) between the TH pin and GND, the influence of extraneous signal can be reduced.

When detecting the coil temperature using an NTC thermistor in particular, the detection temperature may shift to the high temperature side as a result of the effect of the coil signal. It is recommended that  $C_{NTC}$  be connected between the TH pin and GND.

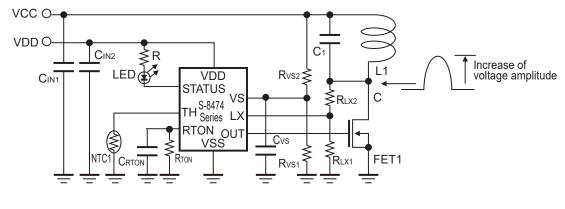


Figure 49

## 7. Precautions

- The usages described in this application note are typical examples using ABLIC Inc. ICs. Perform thorough evaluation before use.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics of the external components should be taken into consideration. ABLIC Inc. bears no responsibility for any patent infringements related to products using the circuits described herein.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement by
  products including this IC of patents owned by a third party.

### 8. Related Sources

Refer to the following datasheets for details of the S-8471 Series and the S-8474 Series.

S-8471 Series Datasheet S-8474 Series Datasheet

The information described herein is subject to change without notice. Please contact our sales representatives for information regarding the latest product version / revision.

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